L508 Hardware Design

LTE Module Series

Version： V1.0.9

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Shanghai Mobiletek Communication Ltd

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1 About this document

1.1 Applicable scope

This document describes the L508 series 4G LTE LCC+LGA Module (hereinafter referred to as L508), the basic specifications, product electrical characteristics, design guidance and hardware interface development guidance. Users need to follow this documentation requirements and guidance for design.

This document applies only to L508 products in the application development.

1.2 Writing purpose

This document provides the design and development basis for the users of the module products. By reading this document, users can have an overall understanding of the product, have a clear understanding of the technical parameters of the product, and on the basis of this document can successfully complete the wireless 4G network functional product or device application development.

This hardware development document not only provides the product functional characteristics and technical parameters, but also provides the product reliability test and related test standards, business function realization process, radio frequency performance index and user circuit design guidance. Is to provide the user with a more comprehensive design reference.

1.3 Support and reference documents list

In addition to this hardware development document, we also provide the product-based Development Board instruction manual and Software Development Instruction Manual, table 1 for the support list.

Table 1 support document list

NO.	Documents
1	《L508 AT Command User Guide》
2	《L508_SPEC.docx》
3	《L508EVBUserManual》
4	《L508 Schematic checklist》
5	《L508 Layout checklist》
6	《L508_Reference Design.pdf》
7	《L508_DECAL.sch》
8	《L508_DECAL.PCB》

1.4 Terms and Abbreviations

Table 2 is the Document relative Terms and Abbreviations

Table 2 Terms and Abbreviation

Abbreviation	Descriptions
ESD	Electro-Static discharge
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver Transmitter
SDCC	Secure Digital Card Controller
USIM	Universal Subscriber Identification Module
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit
PCM	Pulse-coded Modulation
I/O	Input/output
ADC	Analog digital convert

LED	Light Emitting Diode
GPIO	General-purpose Input/Output
GSM	Global Standard for Mobile Communications
GPRS	General Packet Radio Service
CDMA	Code Division Multiple Access
WCDMA	Wideband Code Division Multi Access
UMTS	Universal Mobile Telecommunication System
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
AGPS	Assisted Global Positioning System
BER	Bit Error Rate
DL	Downlink
COEX	WLAM/LTE-ISM coexistence
SMPS	Switched-mode power supplies
LTE	Long Term Evolution
FDD	Frequency Division Duplexing
TDD	Time Division Duplexing

2 Product Overview

This product is an LCC+LGA interface LTE (support to CAT4) wireless communication module, which supports data connection of TDD-LTE/FDD-LTEUMTS/HSDPA/HSPA+/GSM/GPRS/EDGE network. The external size of the module is 30mm×30mm, which can meet almost all M2M and IoT applications, including vehicle tracking, security systems, wireless POS, industrial PDA, intelligent metering, remote maintenance control and so on.

2.1 Main performance

The following table describes the main performance parameters for L508

Table 3 key performance parameter

Performance		**Describe**				
Application processor		1.2GHz Cortex-A7				
Operating System		L508E/L508LA/L508C：RTOS L508TLC：LINUX				
Supply Voltage		Supply Voltage Range 3.2-4.6V, typical supply voltage 3.8V				
Air interface	Support Band	L508E	L508LA (N)*	L508C (N)*	L508TLC (N)*	
	GSM850		√			
	GSM900	√	√	√	√	
	GSM1800	√	√	√	√	
	GSM1900		√			
	WCDMA B1	√	√	√	√	
	WCDMA B2		√			
	WCDMA B4		√			
	WCDMA B5	√	√			

	WCDMA B8	√	√	√	√	
	LTE-FDD B1	√	√	√	√	
	LTE-FDD B2		√			
	LTE-FDD B3	√	√	√	√	
	LTE-FDD B4		√			
	LTE-FDD B5	√	√	√	√	
	LTE-FDD B7	√	√			
	LTE-FDD B8	√	√	√	√	
	LTE-FDD B20	√				
	LTE-FDD B28	√	√			
	LTE-FDD B66		√			
	LTE-TDD B34			√	√	
	LTE-TDD B38	√		√	√	
	LTE-TDD B39			√	√	
	LTE-TDD B40	√	√	√	√	
	LTE-TDD B41	√		√	√	
	Category	CAT4	CAT4	CAT4	CAT4	
	GNSS		√	√	√	
LTE-FDD Characteristic		Uplink up 50Mbps；Downlink up 150Mbps				
HSPA+ Characteristic		WCDMA-HSPA+：Uplink up 5.76Mbps；Downlink up 21Mbps				
UMTS Characteristic		Downlink/Uplink: Downlink up 384Kbps; Uplink up 384Kbps				
GSM Characteristic		EDGE Class 33：Uplink up 236.8Kbps；Downlink up 296Kbps				
		GPRS Class 33：Uplink up 85.6Kbps；Downlink up 107Kbps				
USB		Support USB 2.0 high speed mode，Data transfer rate has a maximum of 480m bps and support OTG				
SIM*1		Support dual voltage（1.8/3.0V），support hot swap function				

SPI*1	general purpose SPI communications and LCD support	
SDIO*2	MMC SDIO interface, support SD, MMC, SDIO, CE-ATA Card Support 1.8/3.0V interface	
	WIFI SDIO interface, support SDIO2.0&3.0 standard Support 1.8V interface	
PCIe	Supports PCIE Gen 1 mode for WIFI interface Max Speed: PCIe Gen 1 (2.5Gbps raw rate)	
Ethernet	Supports 10/100Mbps working mode Support 1.8/3.3V interface	
UART*3	UART1 supports 7-wire interfaces UART2 support 2-wire interface AP_UART, used for software log	
I2C*1	Maximum rat 3.3Mbps	
	I2C signal for open drain output, pull-up resistor in the internal integration	
Audio	Integrated high quality audio codec and audio front end MIC*1 EAR*1	
PCM*1	The PCM signal can be reused as an I2S signal. The PCM corresponds to the I2S signal as follows：	
	I2S Function	PCM Function
	I2S_WS	PCM_SYNC
	I2S_DIN	PCM_DIN
	I2S_DOUT	PCM_DOUT
	I2S_CLK	PCM_CLK
ADC*2	L508E/L508TLC: Resolution 12 bits, voltage detection range 0-1.3 V	

	L508LA/L508C: Voltage detection range 0-1.8 V, temperature drift is large, precision requirements are not high can be used
Antenna interface	Main Antenna, Diversity antenna, GNSS antenna
Physical characteristics	Dimensions L508E/L508LA/L508C: 30mm*30mm*2.5mm L508TLC: 30mm*30mm*2.7mm
Physical characteristics	Encapsulation：LCC+LGA

Note: Some hardware features integrated in L508 devices must be enabled through software. For information about performance features or limitations based on software, see the latest software release notes.

(N) indicates GNSS function. For example, L508CN indicates that the module has GNSS function, while L508C does not. GNSS function will occupy UART2 signal, and UART2 cannot be used when GPS function is available.

2.2 Functional Block Diagram

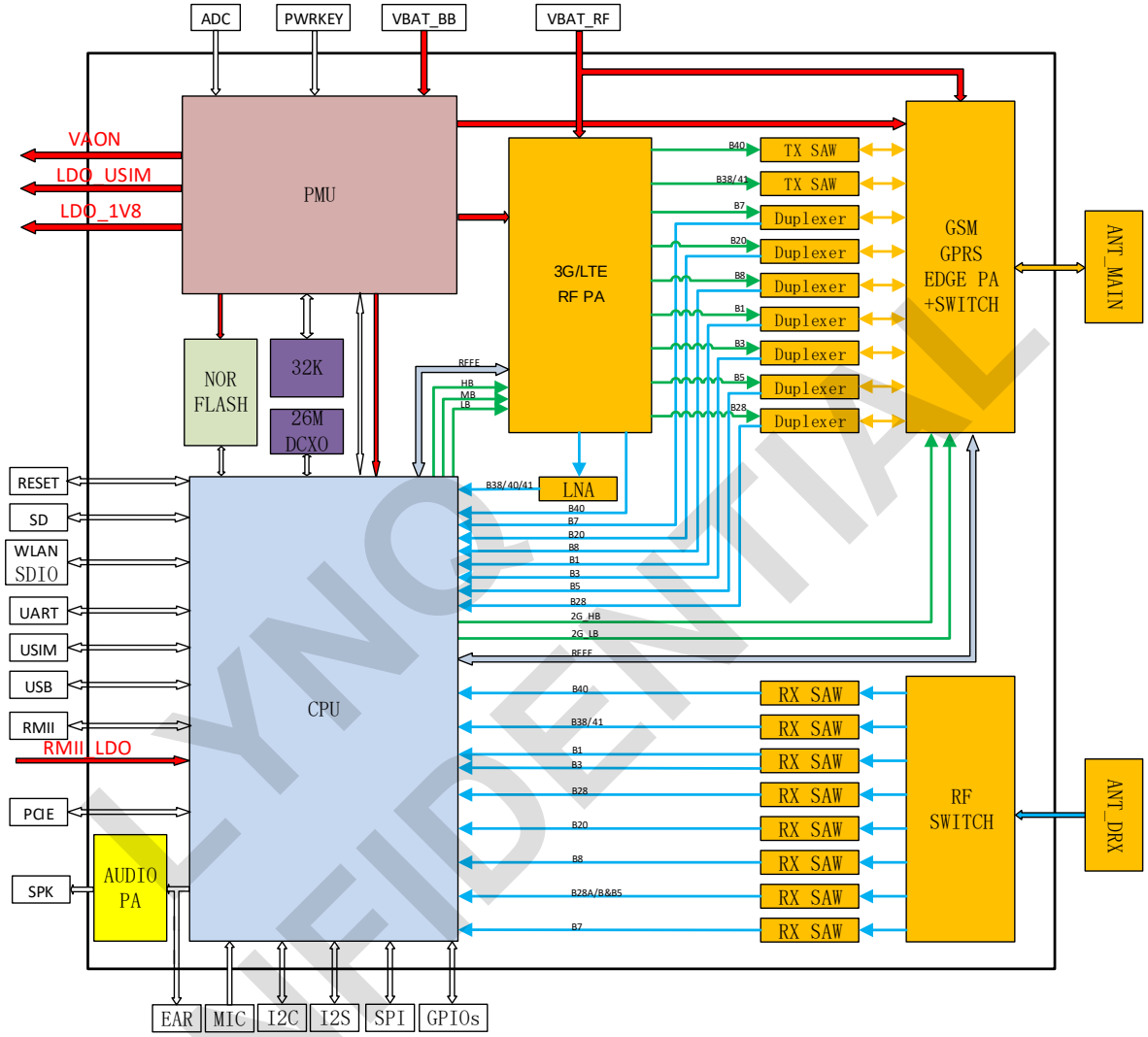


Figure 1 L508E Functional Block Diagram

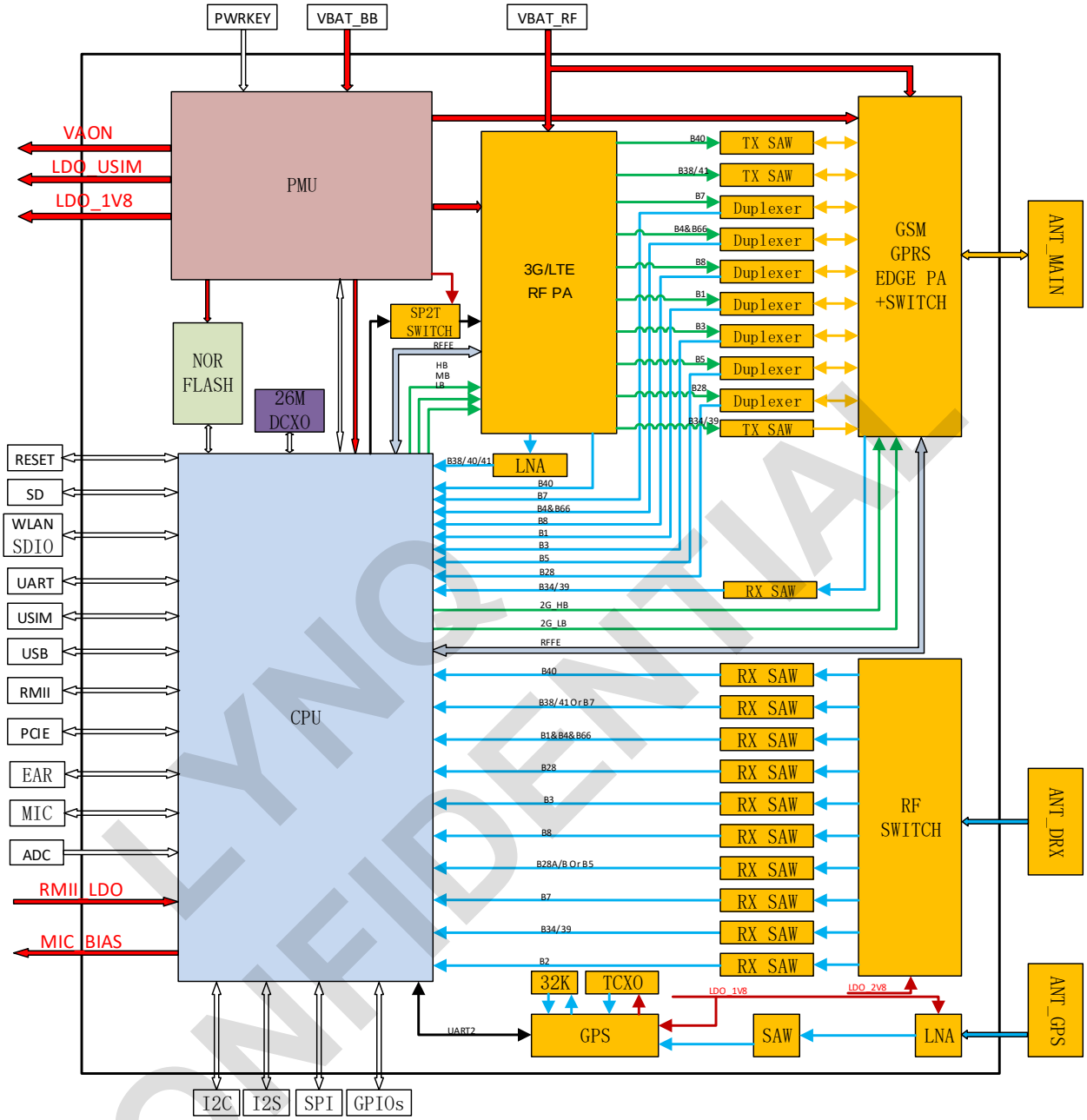


Figure 2 L508LA Functional Block Diagram

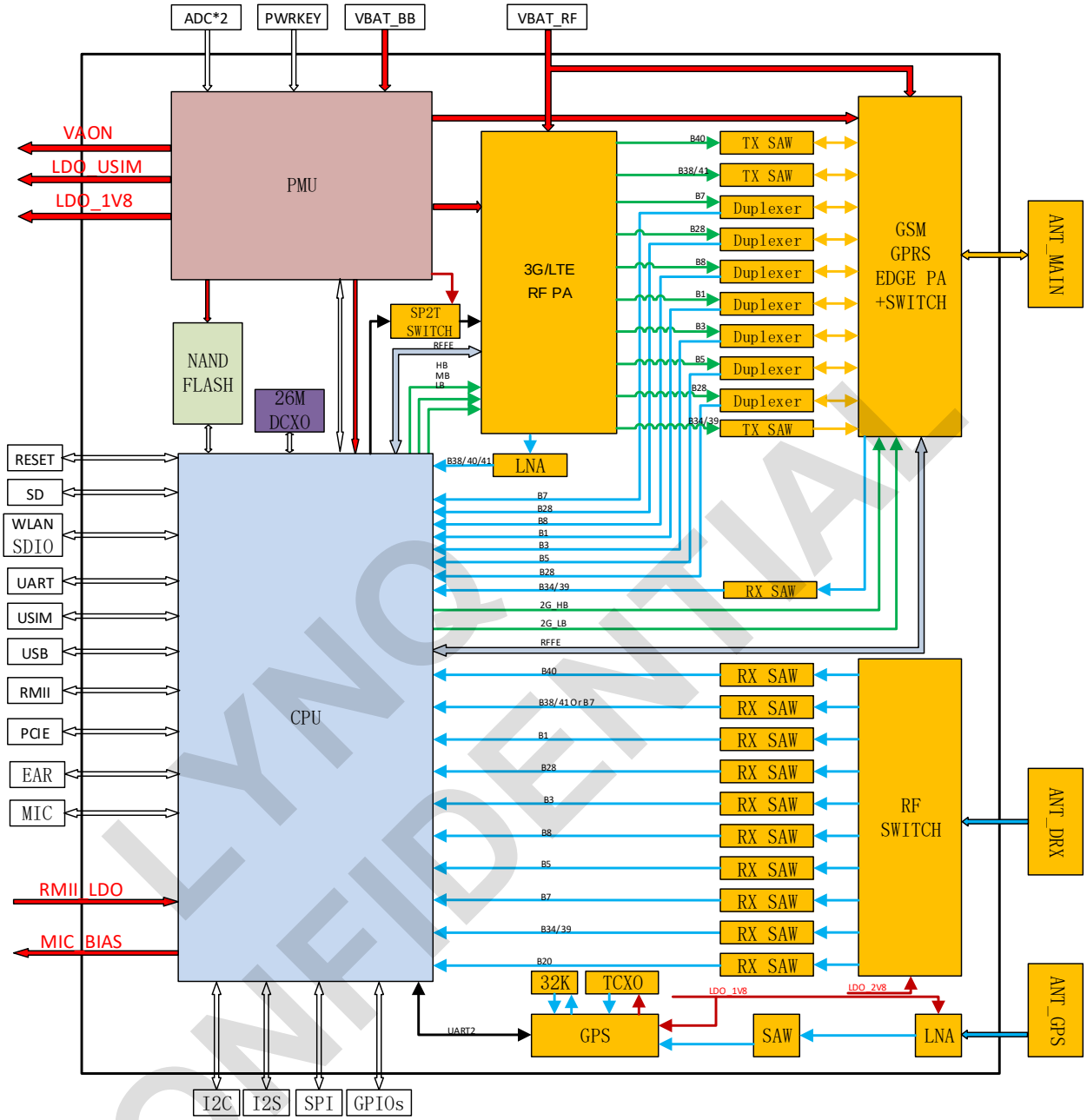


Figure 3 L508LA Functional Block Diagram

2.2.1 Introduction to baseband function

L508 baseband mainly includes the following signal groups: USB Interface, USIM interface, I2C interface, SDIO interface, RMII interface, PCIe interface, UART interface, ADC interface, multiple programmable general input and output, PCM digital audio interface, module boot, module control signal, power and ground.

2.2.2 Introduction to radio frequency function

The working frequency range of the transceiver of this module is shown in Table 4.

Table 4 working frequency band

Working band	Uplink band（Uplink）	Downlink band（Downlink）
GSM850	824 MHz ~849MHz	869 MHz ~894MHz
GSM900	890 MHz ~915MHz	925 MHz ~960MHz
GSM1800	1710 MHz ~1785MHz	1805 MHz~1880MHz
GSM1900	1850 MHz ~1910MHz	1930 MHz~1990MHz
UMTS850	824 MHz ~849MHz	869MHz ~ 894 MHz
UMTS900	890 MHz ~ 915MHz	925 MHz ~ 960 MHz
UMTS1900	1850 MHz ~1910 MHz	1930 MHz ~ 1990 MHz
UMTS2100	1920 MHz ~1980 MHz	2110 MHz ~ 2170 MHz
FDD_LTE B1	1920 MHz~1980 MHz	2110 MHz~2170 MHz
FDD_LTE B2	1850 MHz~1910 MHz	1930 MHz~1990 MHz
FDD_LTE B3	1710 MHz~1785 MHz	1805 MHz~1880 MHz
FDD_LTE B4	1710 MHz~1755 MHz	2110 MHz~2155 MHz
FDD_LTE B5	824 MHz ~ 849MHz	869MHz ~ 894 MHz
FDD_LTE B7	2500 MHz~2570 MHz	2620 MHz~2690 MHz
FDD_LTE B8	880 MHz~915 MHz	925 MHz~960 MHz
FDD_LTE B20	832 MHz~862 MHz	791 MHz~821 MHz
FDD_LTE B28	703MHz~748MHz	758MHz~803 MHz
LTE-TDD B34	2010 MHz~2025 MHz	2010 MHz~2025 MHz
LTE-TDD B38	2570 MHz~2620 MHz	2570 MHz~2620 MHz
LTE-TDD B39	1880 MHz~1920 MHz	1880 MHz~1920 MHz
LTE-TDD B40	2300 MHz~2400 MHz	2300 MHz~2400 MHz
LTE-TDD B41	2535 MHz~2675 MHz	2535 MHz~2675 MHz

GPS L1 BAND		1574.4～1576.44 MHz
GLONASS		1598～1606 MHz
BEIDOU B1		1559.05～1563.14 MHz

Table 5 Conducted transmission power

Working band	Maximum power	Minimum Power
UMTS850	24dBm +1/-3dB	<-50dBm
UMTS900	24dBm +1/-3dB	<-50dBm
UMTS1900	24dBm +1/-3dB	<-50dBm
UMTS2100	24dBm +1/-3dB	<-50dBm
GSM900	33dBm ±2dB	5dBm ± 5dB
DCS1800	30dBm ±2dB	0dBm ± 5dB
GSM900(8-PSK)	27dBm ±3dB	5dBm ± 5dB
DCS1800(8-PSK)	26dBm +3/-4dB	0dBm ± 5dB
FDD_LTE B1	23dBm +/-2.7dB	<-40dBm
FDD_LTE B2	23dBm +/-2.7dB	<-40dBm
FDD_LTE B3	23dBm +/-2.7dB	<-40dBm
FDD_LTE B4	23dBm +/-2.7dB	<-40dBm
FDD_LTE B5	23dBm +/-2.7dB	<-40dBm
FDD_LTE B7	23dBm +/-2.7dB	<-40dBm
FDD_LTE B8	23dBm +/-2.7dB	<-40dBm
FDD_LTE B20	23dBm +/-2.7dB	<-40dBm
FDD_LTE B28	23dBm +/-2.7dB	<-40dBm
TDD_LTE B34	23dBm +/-2.7dB	<-40dBm
TDD_LTE B38	23dBm +/-2.7dB	<-40dBm
TDD_LTE B39	23dBm +/-2.7dB	<-40dBm
TDD_LTE B40	23dBm +/-2.7dB	<-40dBm

TDD_LTE B41	23dBm +/-2.7dB	<-40dBm

Table 6 Conducted reception sensitivity

Working band	Receiving sensitivity (Typical)	Receiving sensitivity (MAX)
WCDMA B1	< -109dBm	3GPP
WCDMA B4	< -109dBm	3GPP
WCDMA B5	< -109dBm	3GPP
WCDMA B5	< -109dBm	3GPP
WCDMA B8	< -109dBm	3GPP
GSM900	< -109dBm	3GPP
DCS1800	< -108dBm	3GPP

Table 7 Reference sensitivity (QPSK)

Bandwidth							
E-UTRA Frequency band	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex mode
1	--	--	TBD	TBD	TBD	TBD	FDD
3	TBD	TBD	TBD	TBD	TBD	TBD	FDD
5	--	--	TBD	TBD	TBD	TBD	FDD
7	--	--	TBD	TBD	TBD	TBD	FDD
8	TBD	TBD	TBD	TBD	--	--	FDD
20	--	--	TBD	TBD	TBD	TBD	FDD
28	TBD	TBD	TBD	TBD	TBD	TBD	TDD
38	TBD	TBD	TBD	TBD	TBD	TBD	TDD
40	TBD	TBD	TBD	TBD	TBD	TBD	TDD
41	TBD	TBD	TBD	TBD	TBD	TBD	TDD

3 Mechanical Dimensions

This module is 135-PIN LCC+LGA packaging module. The package size is 30*30mm. The Pin 1 position is identified by a ground pad with a triangle at the bottom.

3.1 Mechanical Dimensions of Module

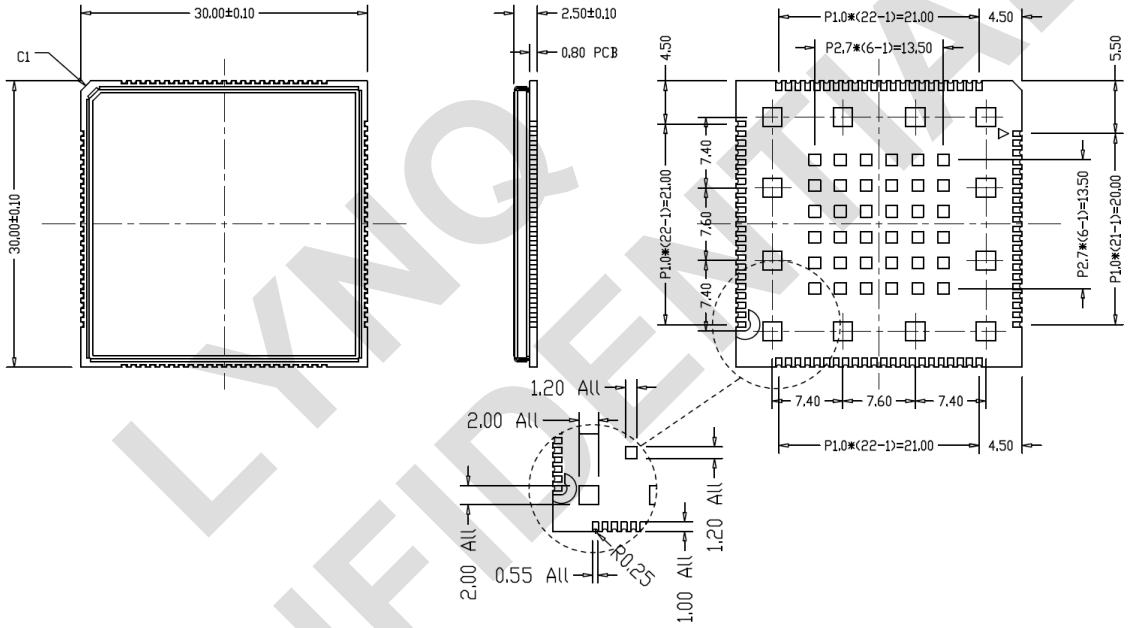


Figure 4 Top, Bottom, Sides Dimensions (Unit: mm)

3.2 Recommended Footprint

The recommended soldering pads are as follows, which can also be obtained directly from our company.

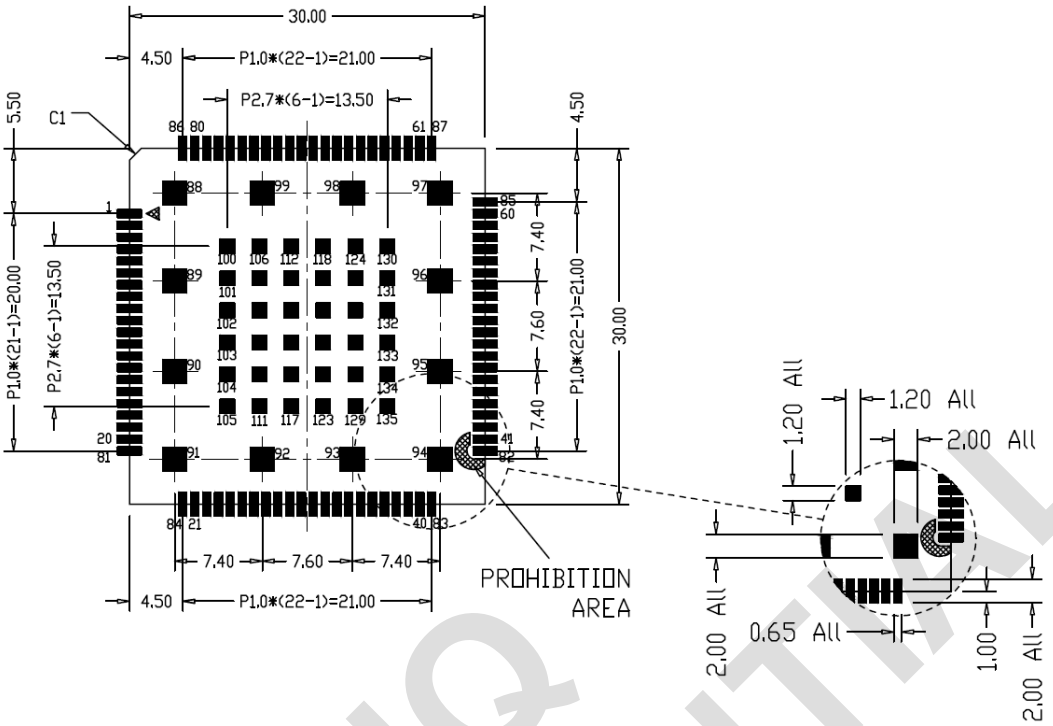
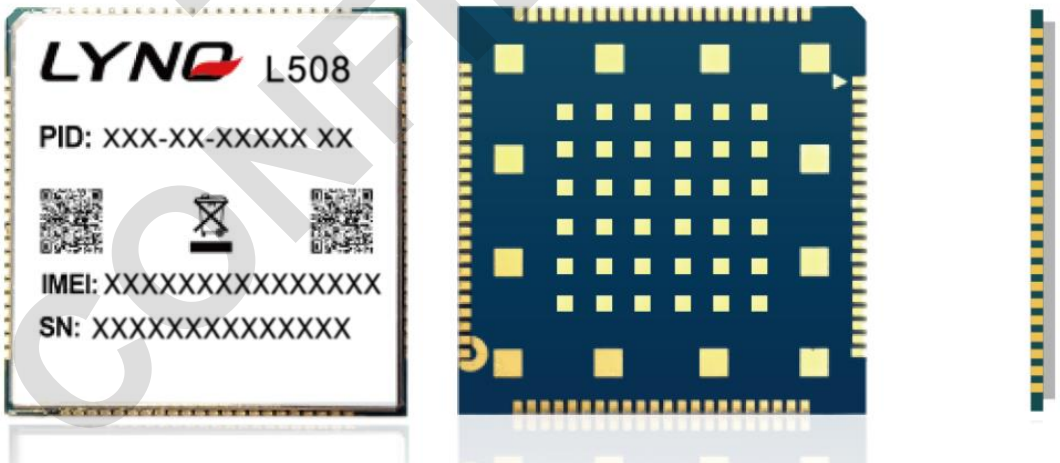


Figure 5 Recommended Footprint (Unit: mm)

3.3 View of the Module



TOP VIEW BOTTOM VIEW SIDE VIEW

Figure 6 View of the Module

4 Interface description

4.1 Pin Definition

4.1.1 Pin I/O parameter definition

The I/O parameter definition for this product is shown in Table 8.

Table 8 I/O parameter definitions

Pin attribute symbol	Description
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
B	Digital Signal input/output
DI	Digital input
DO	Digital signal output
USIM_VDD	SIM card power
RMII_LDO	RMII interface power
B_PD	Digital bidirectional. Default level pull down during system initialization
B_PU	Digital bidirectional. Default level pull up during system initialization
GND	Ground

4.1.2 Pin Layout

All functions of L508 are completed by 135-PIN, please refer to the PIN definition below. The sequence definition of the interface pins of this product is shown in the following figure:

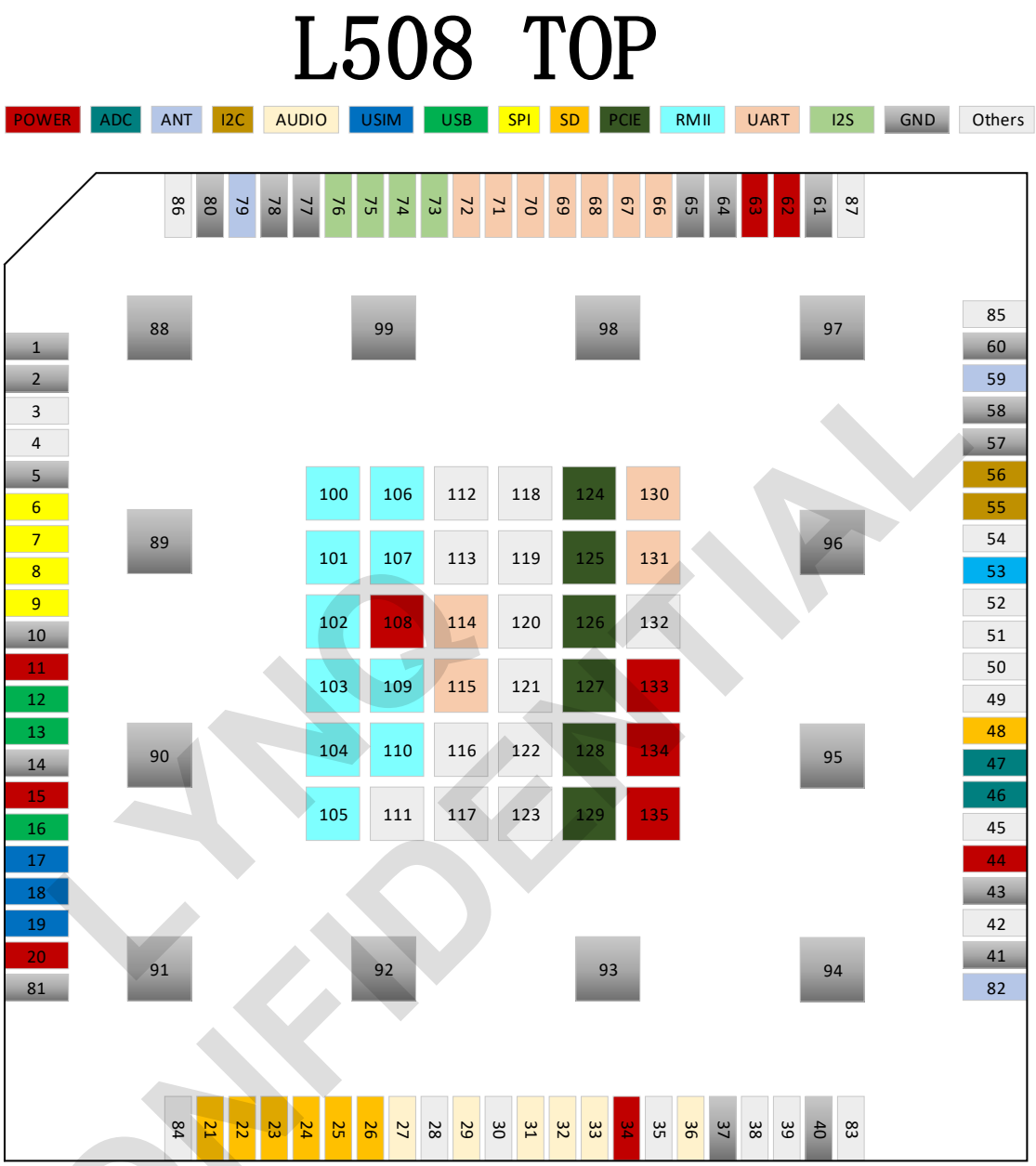


Figure 7 pin configuration (top view)

4.1.3 Pin Description

Table 9 interface definitions

Pin No.	Pin Name	I/O	Voltage domain	Functional description
1	GND	--	--	Ground

2	GND	--	--	Ground
3	EXTON1N	AI	VBAT	Power-on trigger, level trigger (active low)
4	RESET	DI	1.8V	reset input. Active low
5	GND	--	--	Ground
6	SPI_CLK	DO	1.8V	SPI clock
		B_PD		Configurable I/O
7	SPI_MISO	DI	1.8V	SPI input data
		B_PD		Configurable I/O
8	SPI_MOSI	DO	1.8V	SPI output data
		B_PD		Configurable I/O
9	SPI_CS	DO	1.8V	SPI chip select
		B_PD		Configurable I/O
10	GND	--	--	Ground
11	USB_VBUS	PI	VBUS	USB Power input
12	USB_DN	AI, AO	3.3V	USB high-speed data - minus
13	USB_DP	AI, AO	3.3V	USB high-speed data - plus
14	GND	--	--	Ground
15	VDD1V8	PO		LDO for 1/O
16	USB_ID	DI	1.8V	USB high-speed data - ID
17	USIM_DATA	B	1.8V/3V	SIM data line
18	USIM_RST	DO	1.8V/3V	SIM reset control
19	USIM_CLK	DO	1.8V/3V	SIM clock
20	USIM_VDD	PO	1.8V/3V	LDO output for SIM card power
21	MMC_CMD	DO	1.8V/3V	Secure digital controller 1command
22	MMC_DATA0	B	1.8V/3V	Secure digital controller 1 data bit 0
23	MMC_DATA1	B	1.8V/3V	Secure digital controller 1 data bit 1

24	MMC_DATA2	B	1.8V/3V	Secure digital controller 1 data bit 2
25	MMC_DATA3	B	1.8V/3V	Secure digital controller 1 data bit 3
26	MMC_CLK	DO	1.8V/3V	Secure digital controller 1 clock
27	MICN	AI		Microphone negative input
28	GPIO_21	B_PU	1.8V	Configurable I/O
29	MICP	AI		Microphone1 positive input
30	WLAN_PDN	B_PU	1.8V	Configurable I/O
		DO		WLAN chip enable
		DI		RGMII Receive Data 2
31	RECN	AO		Receiver negative output
32	RECP	AO		Receiver positive output
33	RESERVED	--		Reserved for other purposes, Keep it open
34	VDD1V8	PO		LDO output, default voltage is 1.8V
35	32K_OUT	DO	1.8V	32K clock output
36	RESERVED	--		Reserved for other purposes, Keep it open
37	GND	--	--	Ground
38	VBAT_BB	PI		Module baseband main power
39	VBAT_BB	PI		Module baseband main power
40	GND	--	--	Ground
41	GND	--	--	Ground
42	WLAN_DCDC_EN	B_PD	1.8V	Configurable I/O
		DO		WLAN external power enable
43	GND	--	--	Ground
44	SD_LDO	PO	3.0V	LDO output for SD card power, default voltage is 3.0V
45#	GPIO_20	B_PD	1.8V	Configurable I/O, can't pull it up when you boot on

46#	ADC2	AI		L508E: Voltage detection range:0-1.3V L508LA: Voltage detection range:0-1.8V. Accuracy is affected by temperature, can be used when the requirements are not high
47#	ADC1	AI		L508E: Voltage detection range:0-1.3V L508LA: Voltage detection range:0-1.8V. Accuracy is affected by temperature, can be used when the requirements are not high
48	MMC_CD	DI	1.8V	Secure digital card detection
49	STATUS	DO	1.8V	Module status identify: High level power on, low level power off.
		B_PD		Configurable I/O
		DO		RGMII Transmit data 2
50	WAKEUP_IN	DI	1.8V	Interrupt wake up module
		B_PD		Configurable I/O
		DO		RGMII Transmit clock
51	NETLIGHT	DO	1.8V	Identify the system network status
		B_PD		Configurable I/O
		DO		RGMII Transmit data 3
52	WAKEUP_OUT	DO	1.8V	Module external wake up MCU
		B_PU		Configurable I/O
53	USIM_CD	B_PU	1.8V	USIM hot-plug detection (default valid low)
54	FLIGHTMODE	DI	1.8V	The input signal, used to control the system into flight mode, L: flight mode; H: normal mode
		B_PU		Configurable I/O
55	I2C_SCL	DO	1.8V	I2C clock, Internal 4.7K pull up
		B_PU		Configurable I/O

56	I2C_SDA	B_PU	1.8V	I2C data, Internal 4.7K pull up
		B_PU		Configurable I/O
57	GND	--	--	Ground
58	GND	--	--	Ground
59	ANT_DRX	AI		Diversity antenna
60	GND	--	--	Ground
61	GND	--	--	Ground
62	VBAT_RF	PI		Module RF main power
63	VBAT_RF	PI		Module RF main power
64	GND	--	--	Ground
65	GND	--	--	Ground
66	UART_RTS	DO	1.8V	Request to Send
		B_PU		Configurable I/O
67	UART_CTS	DI	1.8V	Clear to send
		B_PU		Configurable I/O
68	UART_RX	DI	1.8V	Receive data, For AT command and data transmission.
		B_PU		Configurable I/O
69	UART_RI	DO	1.8V	Ring indicator
		B_PU		Configurable I/O
70	UART_DCD	DO	1.8V	Data carrier detect
		B_PU		Configurable I/O
71	UART_TX	DO	1.8V	Send data, For AT command and data transmission.
		B_PU		Configurable I/O
72	UART_DTR	DI	1.8V	Data terminal ready (Control module wake or

				sleep)
		B_PU		Configurable I/O
73	PCM_OUT	B_PD	1.8V	PCM output data
		DO		SPI output data
		DI		UART2 clear to send
74	PCM_IN	B_PD	1.8V	PCM input data
		DI		SPI input data
		DI		UART2 request to Send
75	PCM_SYNC	B_PD	1.8V	PCM synchronization signal
		DO		SPI chip select
		DO		UART2 transmit data
76	PCM_CLK	B_PD	1.8V	PCM clock
		DO		SPI clock
		DI		UART2 receive data
77	GND	--	--	Ground
78	GND	--	--	Ground
79#	GNSS_ANT	--	--	L508E: Keep it open
				L508LA: GNSS antenna
80	GND	--	--	Ground
81	GND	--	--	Ground
82	ANT_MAIN	AI，AO		Module main antenna
83	RESERVED	--	--	Reserved for other purposes, Keep it open
84	GPIO_05	B_PU	1.8V	Configurable I/O
		DI		RGMII Receive Data 3
85	DL_KEY	DI		USB Download enable
86	PWRKEY	AI	VBAT	Input pad generally connected to a keypad

				power-on Button. Active low
87	RESERVED	--	--	Reserved for other purposes, Keep it open
LGA PIN				
88	GND	--	--	Ground pad for heat dissipation
89	GND	--	--	Ground pad for heat dissipation
90	GND	--	--	Ground pad for heat dissipation
91	GND	--	--	Ground pad for heat dissipation
92	GND	--	--	Ground pad for heat dissipation
93	GND	--	--	Ground pad for heat dissipation
94	GND	--	--	Ground pad for heat dissipation
95	GND	--	--	Ground pad for heat dissipation
96	GND	--	--	Ground pad for heat dissipation
97	GND	--	--	Ground pad for heat dissipation
98	GND	--	--	Ground pad for heat dissipation
99	GND	--	--	Ground pad for heat dissipation
100	RMII_RX_CTRL	B_PU	RMII_LDO	Collision and Data Valid
101	RMII_RXD0	B_PU	RMII_LDO	Receive Data 0
102	RMII_RXD1	B_PU	RMII_LDO	Receive Data 1
103	RMII_CLK	B_PU	RMII_LDO	Reference clock
104	RMII_TXD0	B_PU	RMII_LDO	Transmit data 0
105	RMII_TXD1	B_PU	RMII_LDO	Transmit data 1

106	RMII_TX_CTRL	B_PD	RMII_LDO	Transmit enable
107	RMII_INT	B_PU	RMII_LDO	RMII interrupt output
108	RMII_LDO	PI		RMII power input (1.8/3.3V)
109	RMII_MDC	B_PD	RMII_LDO	Management clock
110	RMII_MDIO	B_PU	RMII_LDO	Management data I/O
111	RESERVED	--	--	Reserved for other purposes, Keep it open
112	LCD_BK_EN	DO	1.8V	PWM Signal, can be used for backlight
		B_PD		Configurable I/O
113	WIFI_CLK_26M	AO	1.8V	26M clock output
114#	UART2_TX	DO	1.8V	UART2 transmit data
		B_PU		Configurable I/O
115#	UART2_RX	DI	1.8V	UART2 receive data
		B_PU		Configurable I/O
116	WLAN_CLK_REQ	DI	1.8V	WLAN clock request
		B_PD		Configurable I/O
117	WLAN_DAT1	B_PU	1.8V	Secure digital controller 2 data bit 1
118	WLAN_DAT2	B_PU	1.8V	Secure digital controller 2 data bit 2
119	WLAN_CMD	B_PU	1.8V	Secure digital controller 2command
120	WLAN_DAT3	B_PU	1.8V	Secure digital controller 2 data bit 3
121	WLAN_DAT0	B_PU	1.8V	Secure digital controller 2 data bit 0
122	WLAN_CLK	B_PU	1.8V	Secure digital controller 2 clock
123	WLAN_WAKE_HOST	B_PU	1.8V	WLAN interrupt wake up module

124	PCIE_TXP	AIO	0.9V	Differential transmit data signal positive
125	PCIE_TXN	AIO	0.9V	Differential transmit data signal negative
126	PCIE_RXP	AIO	0.9V	Differential receive data signal positive
127	PCIE_RXN	AIO	0.9V	Differential receive data signal negative
128	PCIE_REFCLK_P	AIO	0.9V	Reference clock signal positive
129	PCIE_REFCLK_N	AIO	0.9V	Reference clock signal negative
130	AP_UART_RXD	B_PU	1.8V	Software LOG output
131	AP_UART_TXD	B_PU	1.8V	
132	RESERVED	--	--	Reserved for other purposes, Keep it open
133	RESERVED	--	--	Reserved for other purposes, Keep it open
134	RESERVED	PO		Reserved for other purposes, Keep it open
135	VAON	PO		VRTC power, can be used for GPS backup power

Note: 1, 45PIN, GPIO_20 cannot be pulled up when boot on, which will make the SD card unusable；

2, 46PIN, 47PIN are ADC channel. L508E/L508TLC, Voltage detection range:0-1.3V; L508LA/L508C, Voltage detection range:0-1.8V. L508LA/L508C Accuracy is affected by temperature, can be used when the requirements are not high;

3, 79PIN, L508E no GNSS function, 79PIN can be open processing, 79PIN is GNSS antenna in L508LA/L508C/L508TLC;

4, 114PIN, 115PIN, UART2 signal is used in GNSS function, UART2 can not used when L508LA/L508C/L508TLC has GNSS function;

4.2 Operating conditions

Table 10 operating conditions of module

Description	Functional description	Min	Typ	Max	Unit
USB_VBUS	USB power detect	3.5	5	5.5	V
VBAT	Module main power	3.2	3.8	4.6	V

4.3 Digital logic characteristics

Table 11 Digital I/O characteristics (VDD=1.8V)

Symbols	Description	Min	Typ	Max	Unit
VIH	High-level input voltage	0.7*VDD	VDD	VDD+0.2	V
VIL	Low-level input voltage	-0.3	0	0.3* VDD	V
VOH	High-level output voltage	VDD-0.2	-	VDD	V
VOL	Low-level output voltage	0	0	0.2	V

Note: 1. VDD1V8, USIM (voltage 1.8V), RMII (voltage 1.8V), MMC_SD (1.8V) meet the above characteristics.

2. The internal power supply of I2C, PCM, GPIOS and UART is VDD1V8.

Table 12 Digital I/O characteristics (VDD=3V/3.3V)

Symbols	Description	Min	Typ	Max	Unit
VIH	High-level input voltage	2	VDD	VDD+0.3	V
VIL	Low-level input voltage	-0.3	0	0.8	V
VOH	High-level output voltage	2.4	-	VDD	V
VOL	Low-level output voltage	0	0	0.4	V

Note: 1. USIM (voltage 3.0V), RMII (voltage 3.3V), MMC_SD (3.0V) meet the above characteristics.

2. USIM_CD, MMC1_CD do not support dual voltage, their digital level is 1.8V.

4.4 Power interface

4.4.1 Power pin description

The L508 offers 2 VBAT_BB pins and 2 VBAT_RF pins. VBAT_BB pin is used to supply power to the baseband part and 2G RF PA of the module. VBAT_RF pin is used to supply power to the 3G+4G RF PA inside the module.

The power supply voltage input range of L508 is 3.2V~4.6V, and the recommended value is 3.8V. The performance of VBAT power supply, such as load capacity, ripple size and so on, will directly affect the performance and stability of the module. In the limit case, the module current consumption may reach the instantaneous peak value of about 2A, and there will be voltage sag if the power supply capacity is insufficient. If the voltage drops below 2.7V, the module will be powered down and shut down. Therefore, the user should pay special attention to the design of the power supply part in the design: ensure that even when the module current reaches 2A, the voltage of the VBAT fall behind cannot be lower than 2.7V. If the voltage drops below 2.7V, the module will power down and shut down.

The following are the power supply characteristics of the module during normal operation:

Table 13 definition and description of power supply

Pin No.	Pin Name	Functional description	DC Characteristics (V)		
			Min	Typ	Max
38,39	VBAT_BB	Module baseband main power	3.2	3.8	4.6
62,63	VBAT_RF	Module RF main power	3.2	3.8	4.6
IVBAT(peak)	Module GPRS, EDGE mode peak current		-	TBD	-
IVBAT(peak)	Module CAT-4 mode peak current		-	TBD	-

4.4.2 Power requirement

VBAT_BB, VBAT_RF drive baseband and RF PA chip respectively, in order to ensure VBAT_BB, VBAT_RF voltage does not drop below 2.7V, near module, suggested to parallel a 100 uf tantalum capacitance, low ESR and 100nF, 33nF and 10nF filter capacitance, and suggested PCB go line short and wide enough, as far as possible in order to reduce the equivalent impedance of VBAT go line, to ensure maximum transmitted power, voltage is no voltage drop. It is recommended that VBAT_BB PCB trace width should not be less than 2mm and VBAT_RF PCB trace width should not be less than 1.5mm. And the longer the line, the wider the line width, the power supply part of the ground plane as complete as possible.

In order to suppress the power fluctuation impact and ensure the stability of the output power supply, it is recommended to add a TVS tube with rated power above 0.5W at the front end of the power supply and place it near the VBAT end of the module to play the role of surge protection. The reference circuit is as follows:

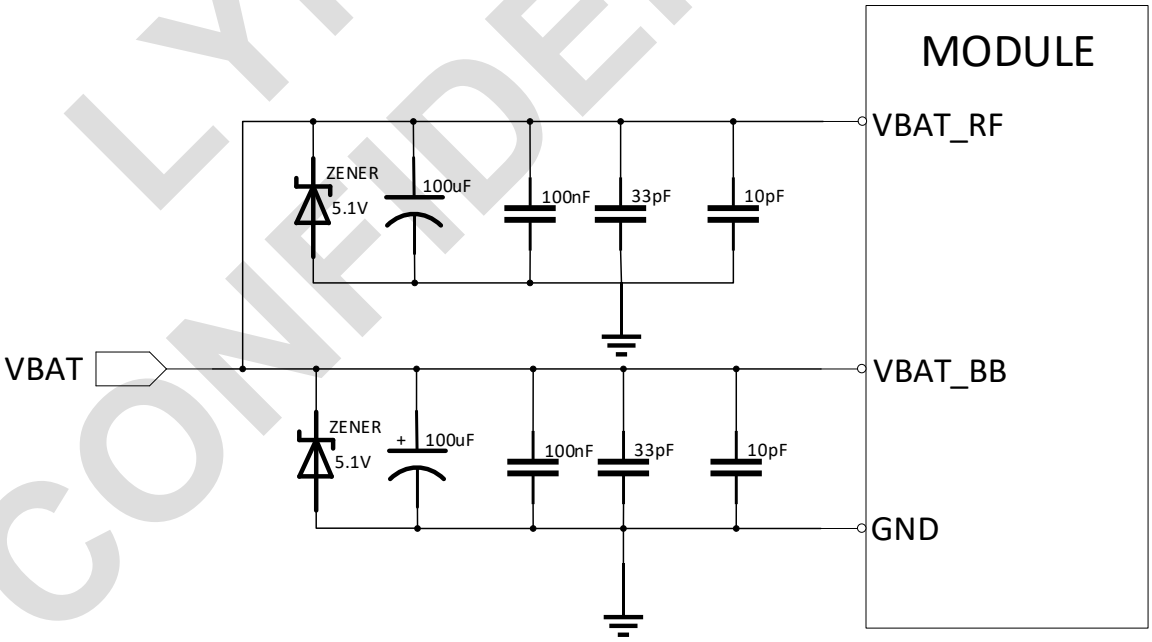


Figure 8 Power interface recommendation circuit

Table 14 Power Zener diode recommended

NO.	Manufacturer	Part Number	Power	Package

1	On semi	MMSZ5231BT1G	500mW	SOD123
2	Prisemi	PZ3D4V2H	500mW	SOD323
3	Vishay	MMSZ4689-V	500mW	SOD123
4	Crownpo	CDZ55C5V1SM	500mW	0805

4.4.3 Power Supply Design Guide

If the voltage difference is not big, can use "power supply scheme". LDO requires over-current capacity of more than 2A, but because LDO is a linear buck, its transient response capacity is poor, and the front and rear terminals need to be equipped with a large amount of capacitance, to prevent GSM high-power transmission when the voltage fluctuation is too large, may lead to reset or shutdown. Output voltage to be controlled at 3.8V.

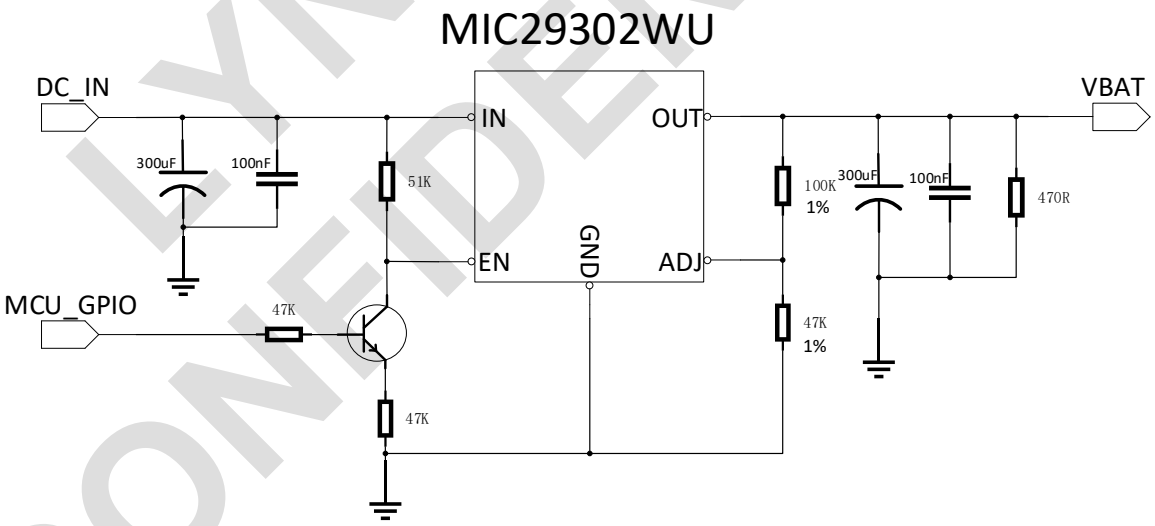


Figure 9 Recommended LDO power supply circuit

If the voltage difference is large, it is recommended to use DC/DC, the output current requirements of more than 2A, such as figure 4-5 using DC switching power supply, supplemented by a large capacity (more than 330 UF) , to ensure the normal operation of RF PA (power amplifier) , provides sufficient transient current in GSM Burst mode. The advantage of the reference design is that it can provide

better transient current response, meet the working requirement of the module under the weak signal of 2G, and prevent the network drop or port restart caused by power shortage.

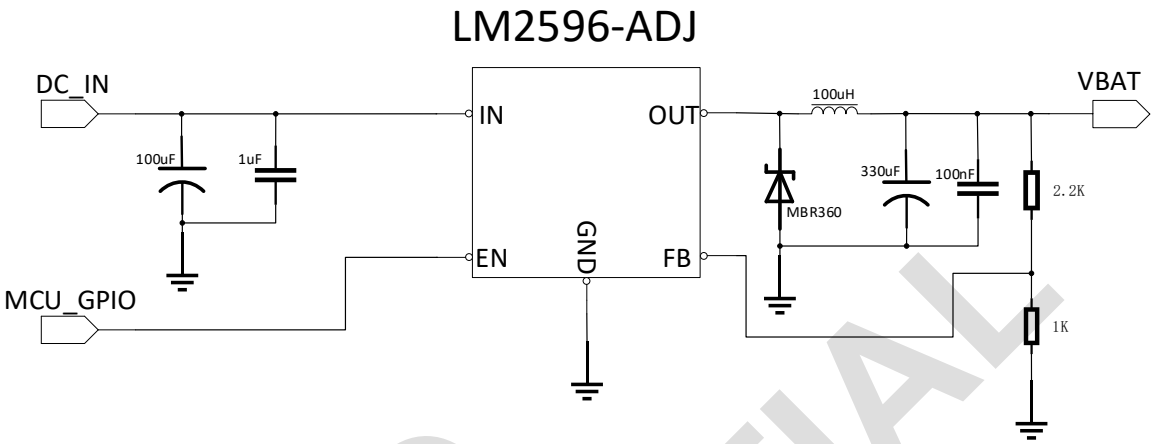


Figure 10 Recommended DC/DC power supply circuit

4.4.4 Charging circuit design reference

The module has reserved the charging interface. If you want to realize the charging function, you can refer to the following charging circuit

Table 15 Charging interface definition

Pin No.	Pin Name	I/O	Functional description
11	USB_VBUS	PI	USB power detect
15	VDD1V8	PO	LDO for I/O
45	GPIO_20	B_PD	Charging chip enable, active low
46	ADC2	AI	Battery NTC temperature detection
47	ADC1	AI	Battery voltage detection
84	GPIO_05	B_PU	Charging state detection
86	EXTON1N	AI	Charging startup detection, charging module startup

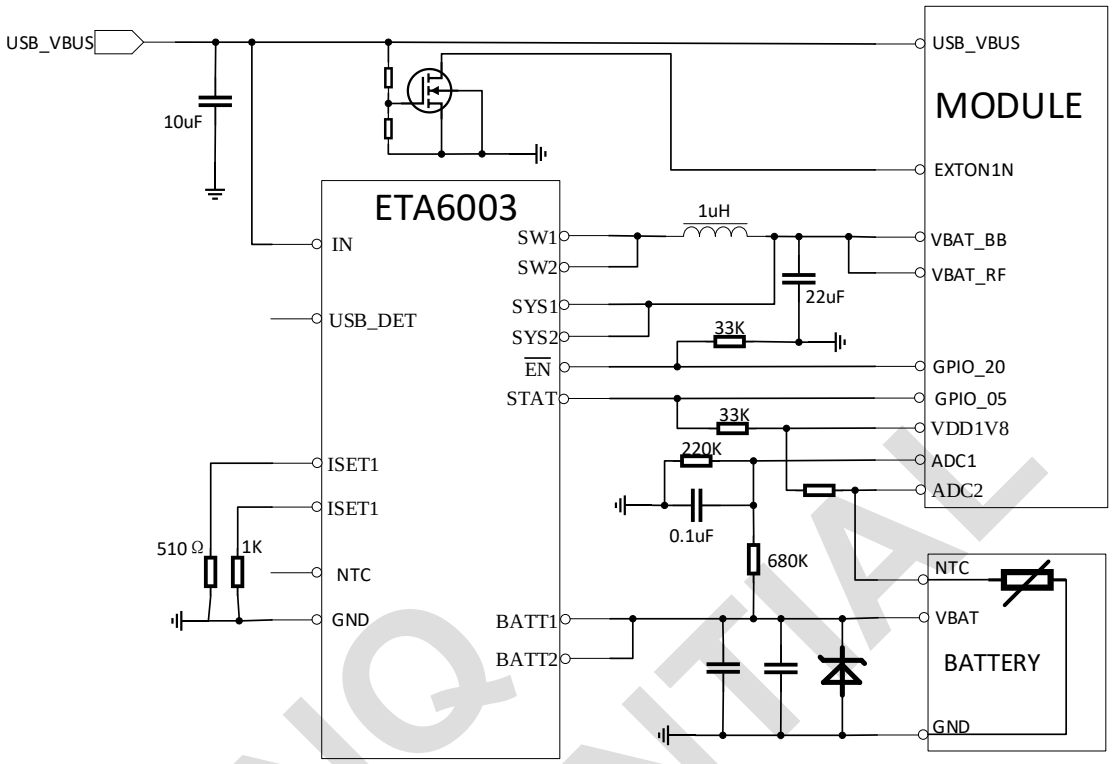


Figure 11 Charging reference circuit

4.5 USIM card interface

4.5.1 Pin Description

The L508 module baseband processor integrates an ISO 7816-2 Compliant Sim card interface that supports and automatically detects 3.0 V and 1.8 V SIM cards, and the USIM card interface signal is shown as shown below.

Table 16 SIM Card interface definition

Pin No.	Pin Name	Functional description	Further description
20	USIM_VDD	LDO output for SIM card power	USIM card power supply, output by the module, support 1.8v/3v dual voltage range.
17	USIM_DATA	SIM data line	USIM card DATA signal, two-way signal, supports 1.8V/3V dual voltage range.

18	USIM_RST	SIM reset control	USIM card reset signal, output by the module, support 1.8v/3v dual voltage range.
19	USIM_CLK	SIM clock	USIM card clock signal, output by the module, supports 1.8V/3V dual voltage range.
53	USIM_CD	USIM hot-plug detection	Only 1.8 v Range is supported.

Note: L508 SIM Card Channel Signals support dual-level mode, the module will automatically adapt to the type of External Sim card jump.

4.5.2 Electrical characteristics

The USIM Card Signal Unit, on the line near the USIM card seat, please note the need to add ESD protection devices when designing.

In order to meet the requirements of 3GPP TS 51.010-1 protocol and EMC certification, it is recommended that the seat of the USIM card should be placed near the interface of the module USIM card, so as to avoid the serious distortion of the waveform caused by the long line and the influence of the Signal integrity. USIM and USIM signal routing recommendations packet earth protection. A 100nF and a 33pF capacitor are connected in parallel between the GND and the SIM_VDD. A 22pF capacitor is connected in parallel between the USIM, USIM, USIM and the GND to filter out interference from the RF signal. USIM, USIM, USIM series 22 resistance to enhance static protection.

4.5.3 USIM card interface application

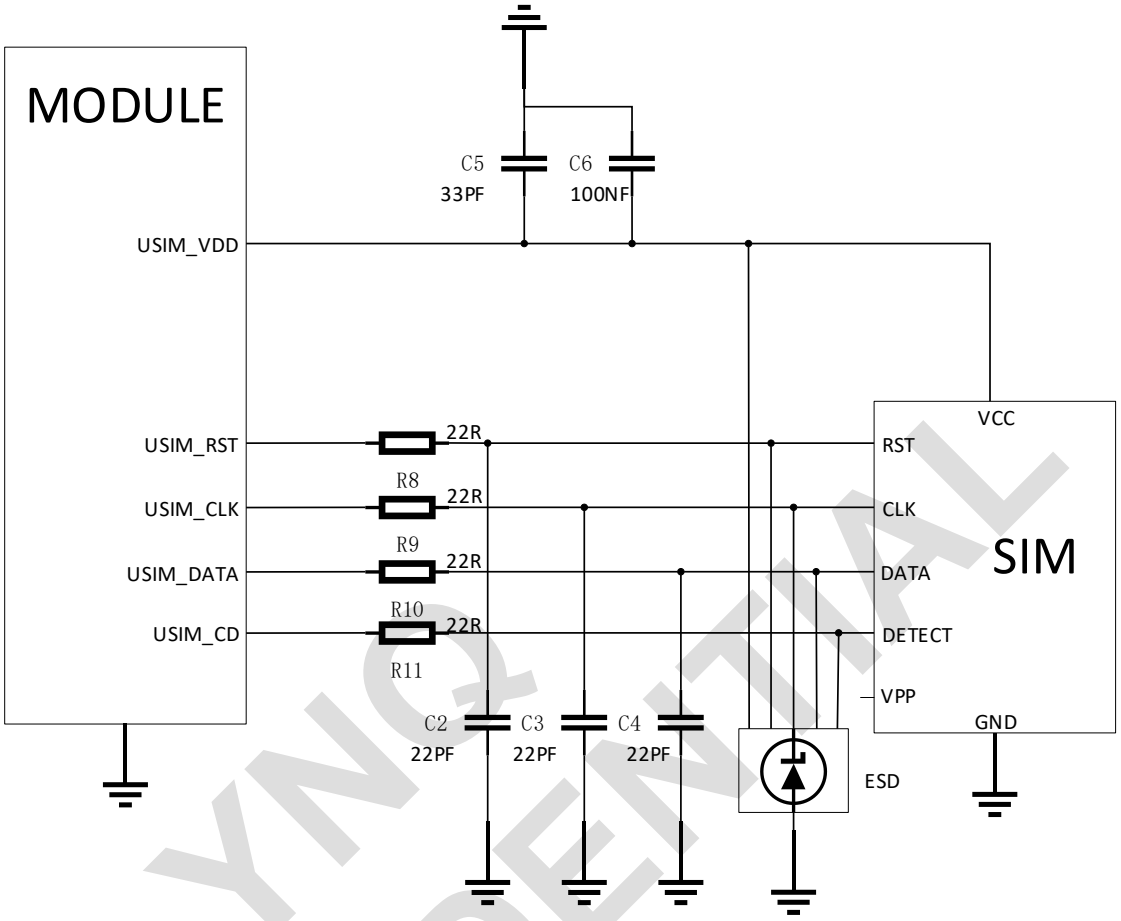


Figure 12 SIM Card Signal Connection Circuit

Note: 1. The pull-up resistors on the USIM signal lines have been designed in the module without the need to add the pull-up resistors in the peripheral circuit design.

2. The L508 supports a hot-swap design, so if you don't need one, just leave the SIM empty.

4.6 PCM interface

4.6.1 Pin Description

The L508 module provides a digital audio interface (PCM) to transmit digital voice signals as the PCM main device. The Pin signals are shown in the following table:

Table 17 PCM signal interface definition

Pin No.	Pin Name	Functional description
73	PCM_OUT	PCM data output
74	PCM_IN	PCM Data input
75	PCM_SYNC	PCM synchronization signal
76	PCM_CLK	PCM Data clock

4.6.2 PCM timing

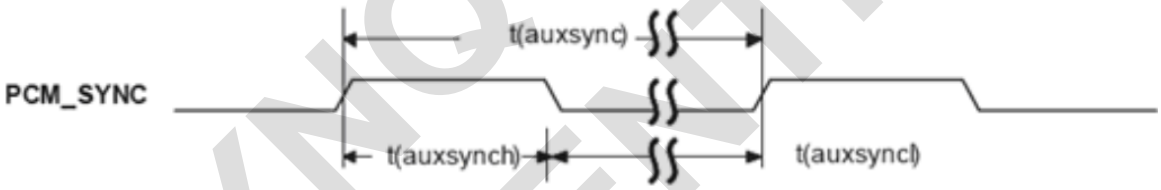


Figure 13 PCM timing

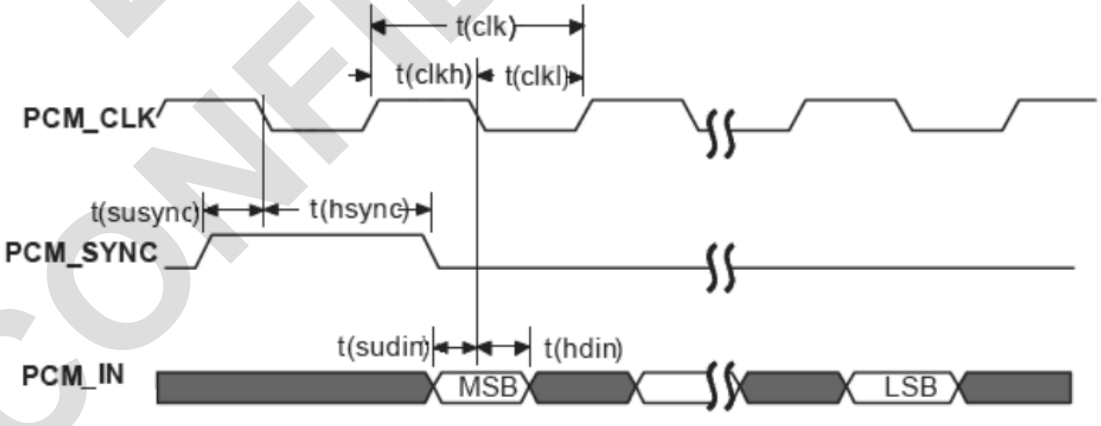


Figure 14 Timing of external CODEC to module

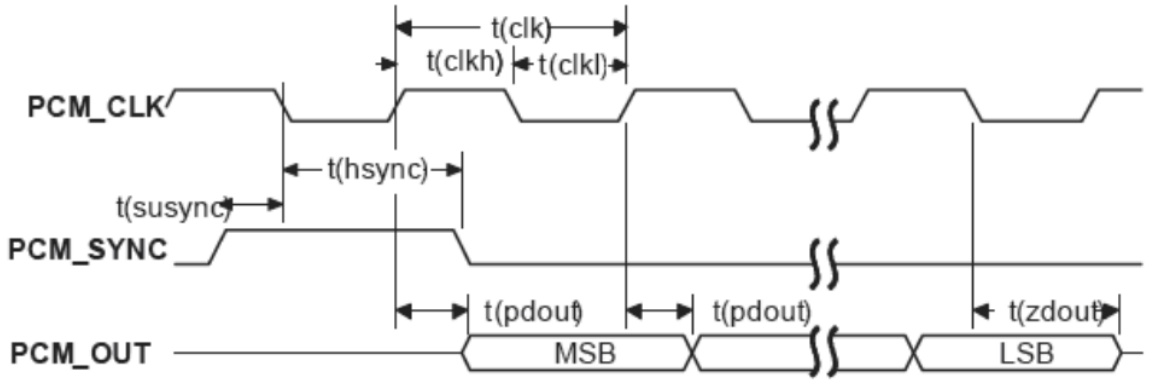


Figure 15 Timing of the external CODEC for the module

4.6.3 PCM interface application

In use, L508 module can only be used as the main device, PCM_SYNC, PCM_CLK are used as the output pin, PCM_SYNC output 8kHz synchronous signal, PCM Data support 8bit or 16bit Data format. And the CODEC connection from the device is shown below:

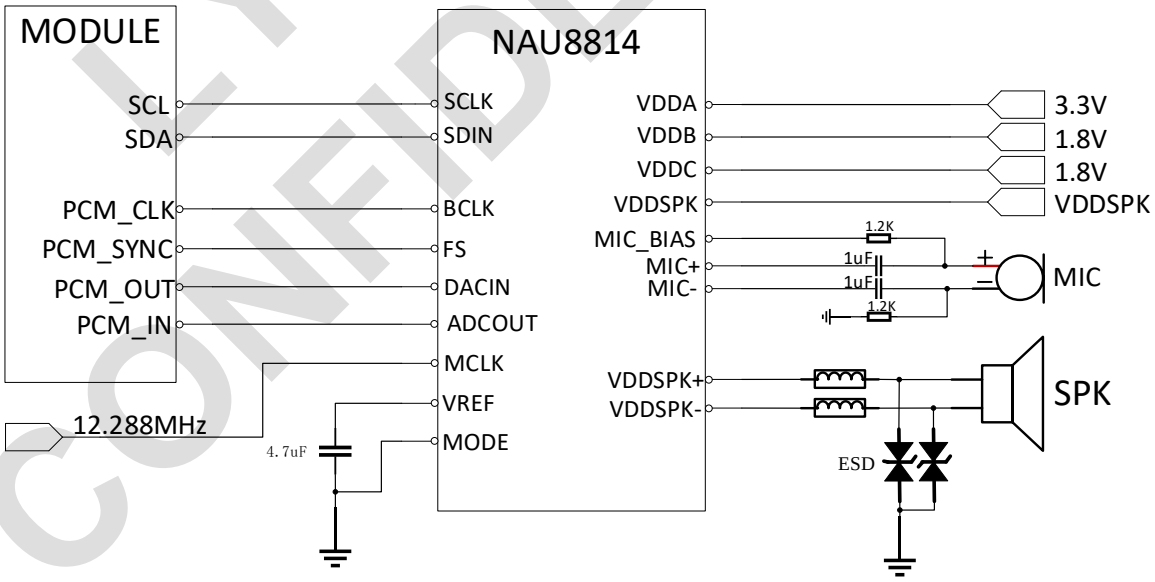


Figure 16 PCM Application Circuit (L508 module as the main PCB device)

Note: 1, when the PCM chip is connected, the electrical characteristics of the PCM interface should strictly refer to the range of high and low levels of digital signals.

2, the master clock of the PCM chip needs to be supplied by the External Crystal Oscillator, the specific design requirements can be obtained from our marketing department related documents.

3.NAU8814 is the default support for L508 as the PCM decoder chip. See L508 reference design for more details

4.7 USB2.0 interface

4.7.1 Pin Description

The product has a high-speed USB2.0 interface, supporting low-speed, full-speed and high-speed mode, the main processor (AP) and the module between the main USB interface for data transmission. The interface definition of USB is given in Table 19.

Table 18 USB interface definitions

Pin No.	Pin Name	Functional description	DC Characteristics (V)		
			Min	Typ	Max
11	USB_VBUS	USB Power input	3.5V	5V	5.5V
12	USB_DN	USB high-speed data - minus	-	-	-
13	USB_DP	USB high-speed data - plus	-	-	-
16	USB_ID	USB high-speed data - ID	--	1.8V	--

4.7.2 USB interface application

USB Bus is mainly used for data transmission, software upgrade, module program detection. If the USB circuit works in high speed mode, if the ESD design is needed, the junction capacitance value of ESD Protection Device<2PF must be satisfied, otherwise the large junction capacitance will cause waveform distortion and affect the bus communication. The differential impedance of the differential data line should be controlled at 90ohm±10%. The application is illustrated in the following figure:

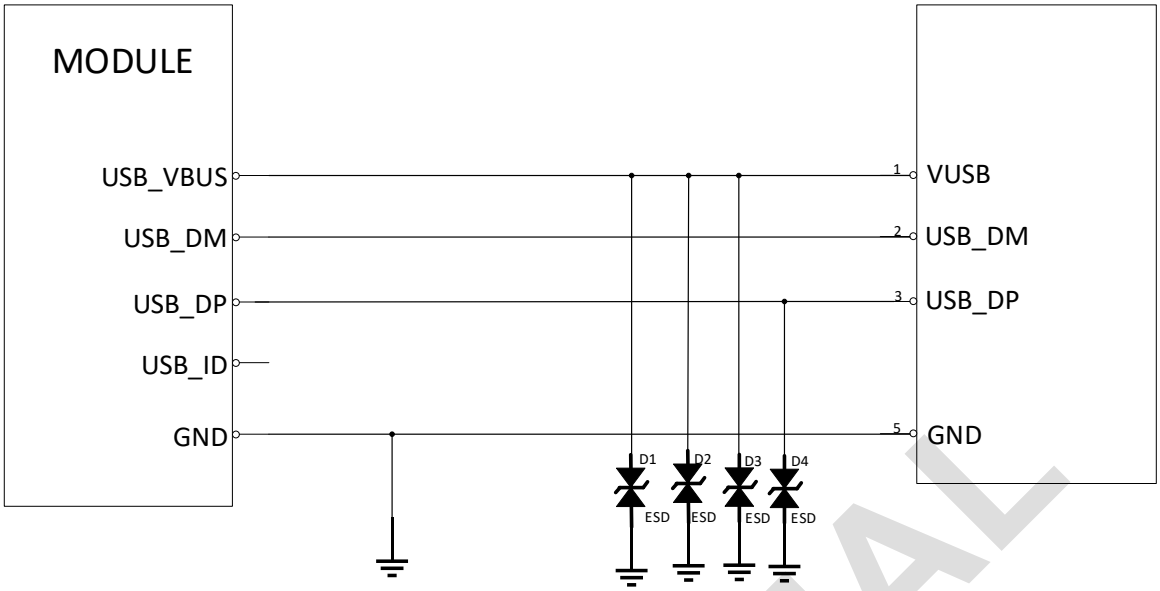


Figure 17 USB application circuit

4.8 UART interface

4.8.1 Pin Description

The L508 module provides 2 serial communication interfaces, UART as a complete asynchronous communication interface, supports the signal control of Standard Modem handshake signal, and accords with RS-232 interface protocol, also support 4-wire serial bus interface or 2-wire serial bus interface mode, the module can be UART interface for serial communication and AT instruction input, etc.

These UART ports support programmable data widths, programmable data stop bits, programmable parity bit, have separate TX and RX FIFOs. The depth of the TX FIFO is 64 bytes and the width is 8bits.The RX FIFO has a depth of 64 bytes and a width of 11bits

Pin Signal definitions are shown in the following table.

Table 19 UART interface definitions

Pin No.	Pin Name	I / O type	Functional description

66	UART_RTS	DO	Request to Send
67	UART_CTS	DI	Clear to send
68	UART_RX	DI	Receive data, For AT command and data transmission.
69	UART_RI	DO	Ring indicator
70	UART_DCD	DO	Data carrier detect
71	UART_TX	DO	Send data, For AT command and data transmission.
72	UART_DTR	DI	Data terminal ready (Control module wake or sleep)
114#	UART2_TX	DO	UART2 transmit data
115#	UART2_RX	DI	UART2 receive data

Note: UART2 signal can be used in GNSS function, UART2 can not be used for other purposes when L508LA/L508C/L508TLC has GNSS function.

4.8.2 UART interface application

The UART can be connected in full RS232 mode, 4-wire mode or 2-wire mode if it is used in communication between module and application processor and the level is 1.8V matching.

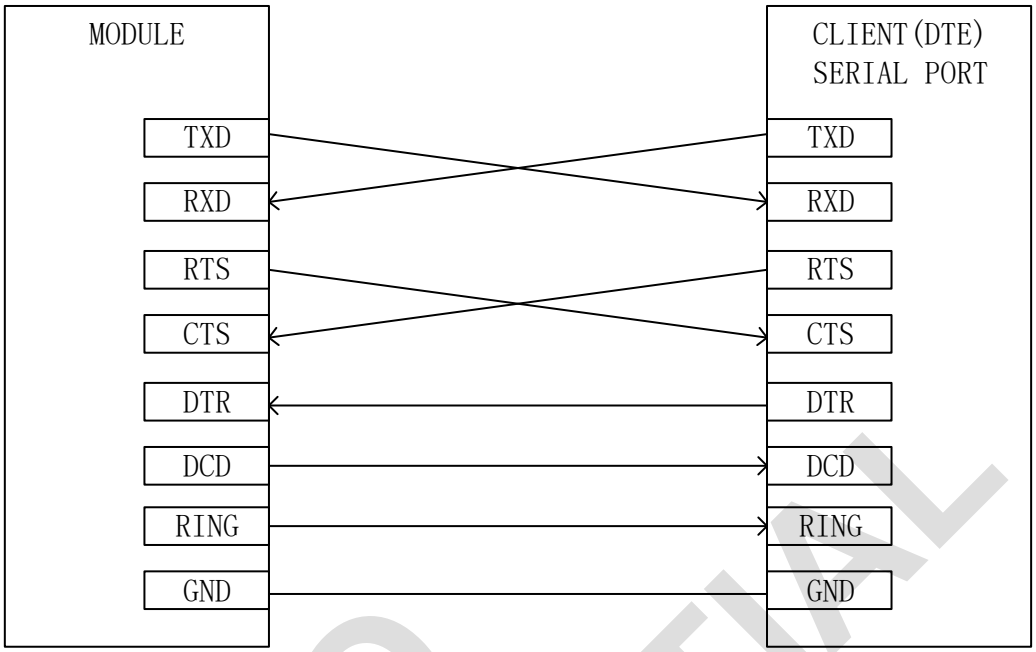


Figure 18 Module serial port and AP application processor full function connection method

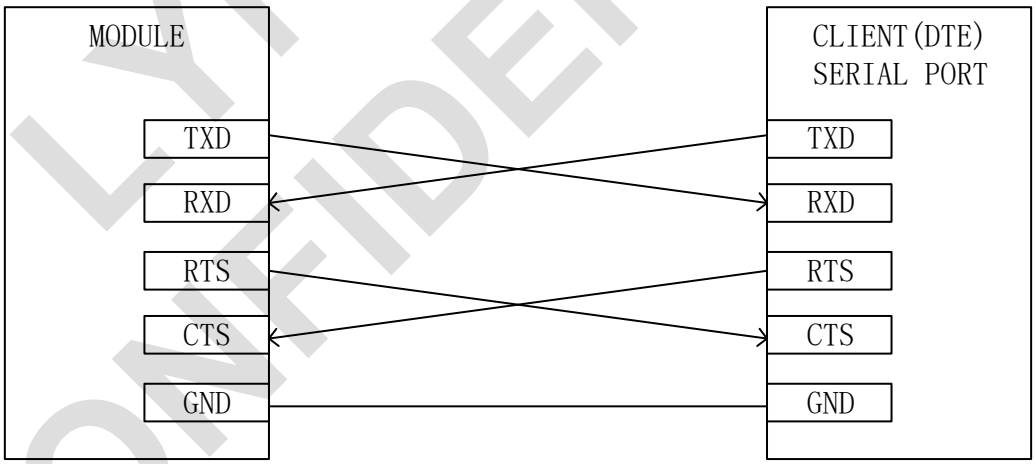


Figure 19 Module serial port and application processor 4-wire connection

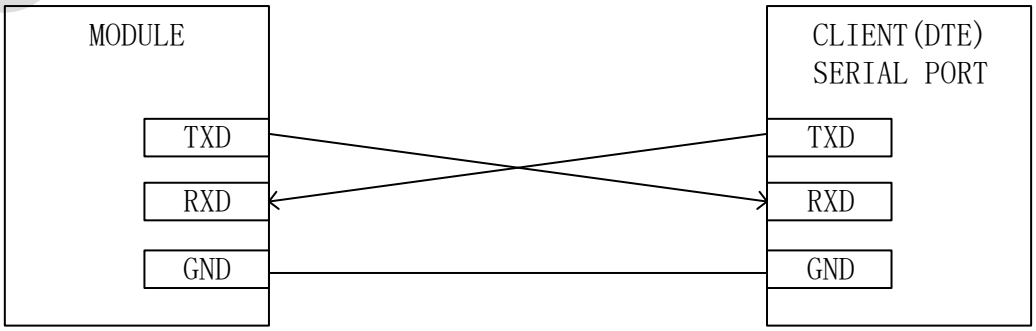


Figure 20 Module serial port and AP application processor 2-wire connection

Module interface level is 1.8 v, if the AP interface level does not match, it is recommended to add level conversion circuit.

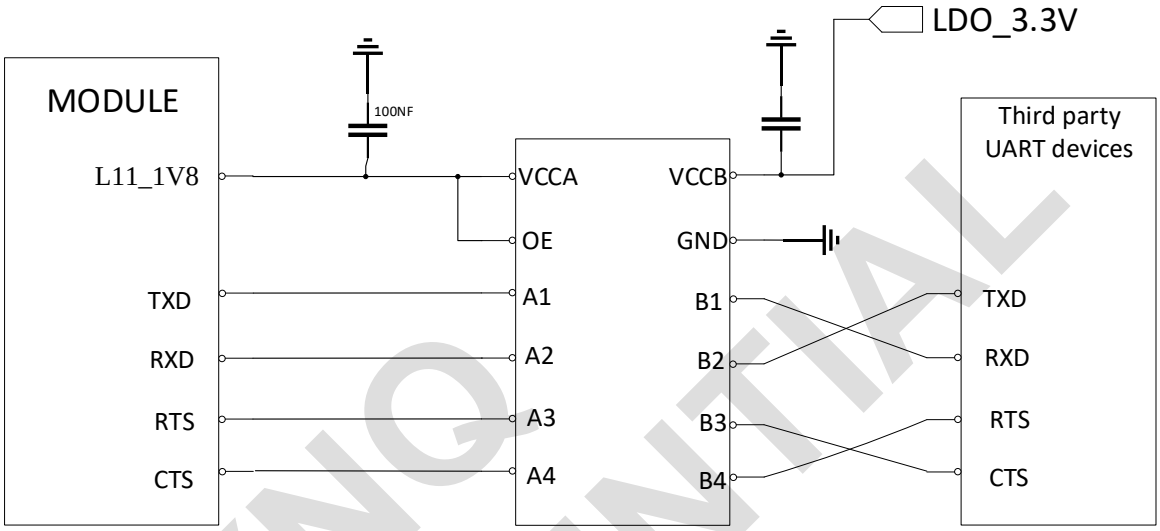


Figure 21 UART level transition connection diagram

When the module communicates with PC, the RS232 level conversion circuit needs to be added between the module and PC because its serial port is 1.8V CMOS level. Recommended customers to use SN65C3238, for the application of the chip see chip specifications. The customer needs to ensure that the level converter chip is connected to the module with an i/o voltage of 1.8 v.

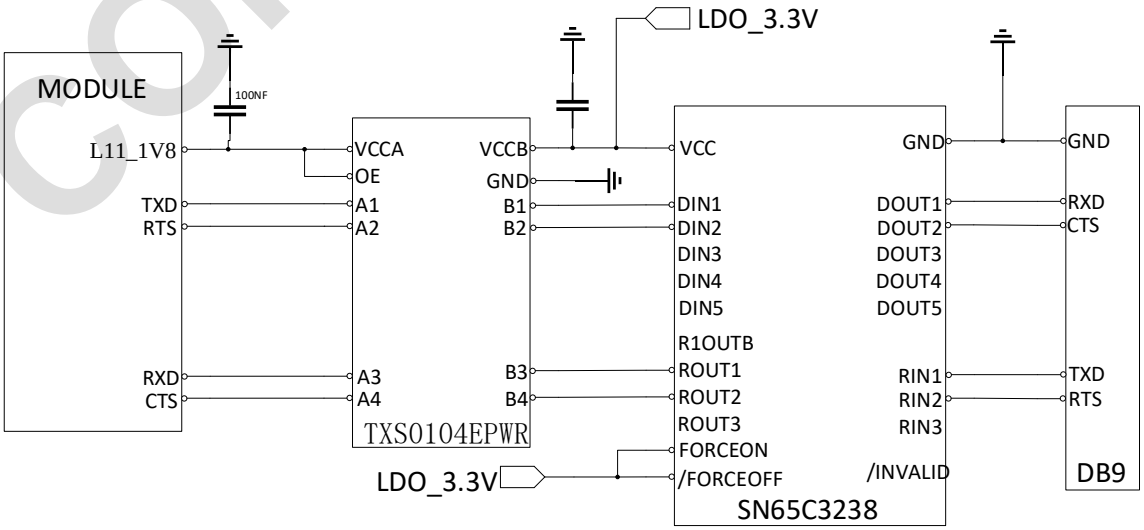


Figure 22 UART to RS232 reference circuit

4.9 SPI interface

4.9.1 Pin Description

L508 module provides two sets of SPI interface, as the main device, SPI signal frequency up to 52MHz, wherein 6-9 PIN can be displayed by SPI LCD. SPI interface signals are shown in the following table.

Table 20 SPI interface definitions

Pin No.	Pin Name	I / O type	Functional description
6	SPI_CLK	DO	SPI clock
7	SPI_MISO	DI	SPI input data
8	SPI_MOSI	DO	SPI output data
9	SPI_CS	DO	SPI chip select
73	PCM_OUT	DO	SPI output data
74	PCM_IN	DI	SPI input data
75	PCM_SYNC	DO	SPI chip select
76	PCM_CLK	DO	SPI clock

4.9.2 SPI reference design

The voltage range of SPI serial port is 1.8V.

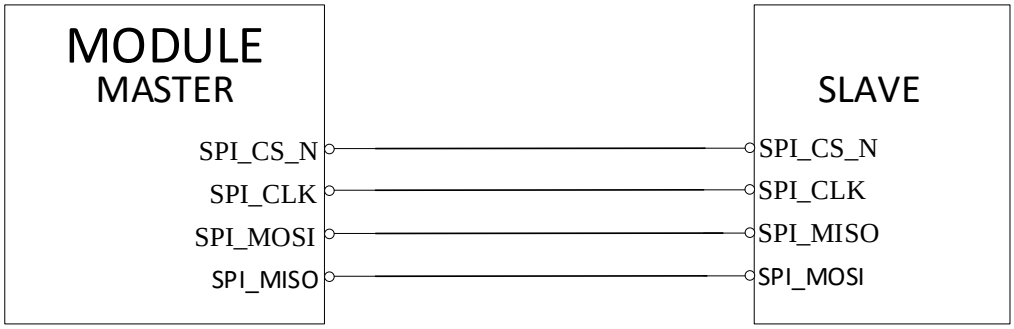


Figure 23 SPI connection diagram 1

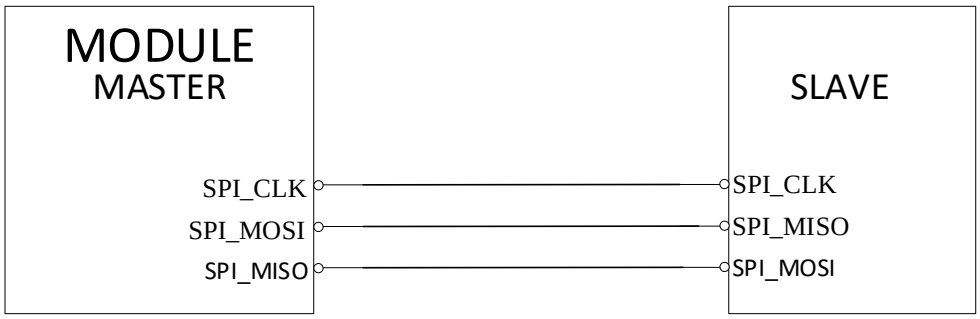


Figure 24 SPI connection diagram 2

4.9.3 LCD reference design

The L508's SPI signal supports both 4-wire 8bit and 3-wire 9bit LCD. The maximum resolution is dependent on the frame rate of the LCD, and the maximum frame rate supported by a 240×320 screen is about 18fps.

Table 21 LCD interface definitions

Pin No.	Pin Name	I / O type	Functional description
6	SPI_CLK	DO	SPI clock
8	SPI_MOSI	DO	SPI output data
9	SPI_CS	DO	SPI chip select
70	UART_DCD	DO	LCD reset signal
72	UART_DTR	DO	LCD data/command (D/CX)
112	LCD_BK_EN	DO	PWM for LCD backlight

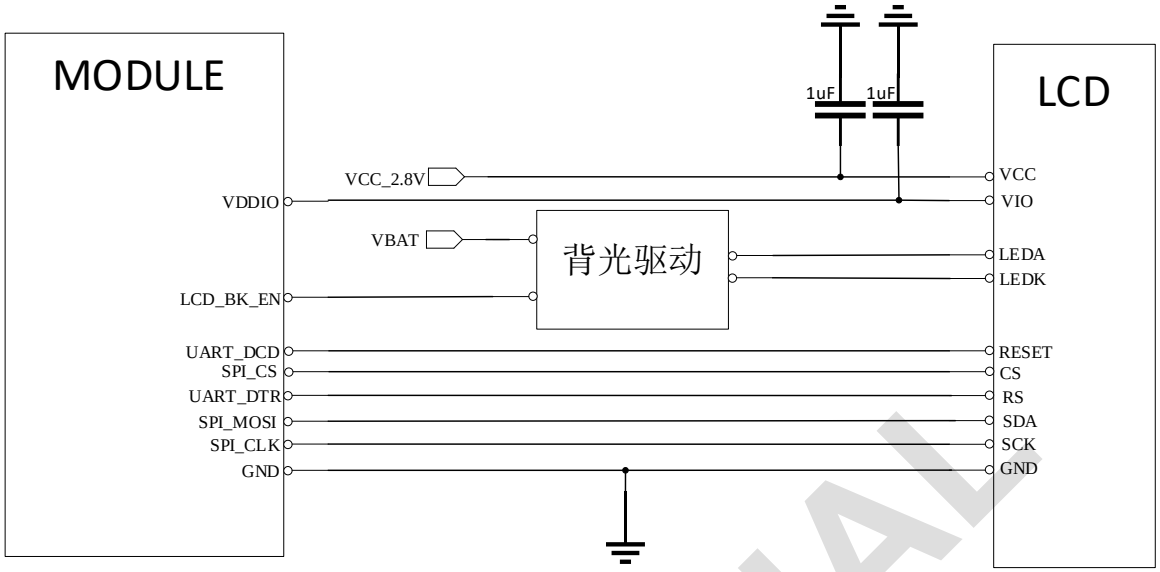


Figure 25 LCD reference design

4.10 I2C interface

The control interface of I2C used to communicate with peripheral devices, SDA and SCL are two-way communication lines, running voltage is 1.8 v, high-speed mode transmission rate can reach 3.3Mbps, since the internal L508 has done the pull-up of I2C interface, so the external pull-up design is not needed.

Table 22 I2C interface definitions

Pin No.	Pin Name	I / O type	Functional description
55	I2C_SCL	B_PU	I2C clock, Internal 4.7K pull up
56	I2C_SDA	B_PU	I2C data, Internal 4.7K pull up

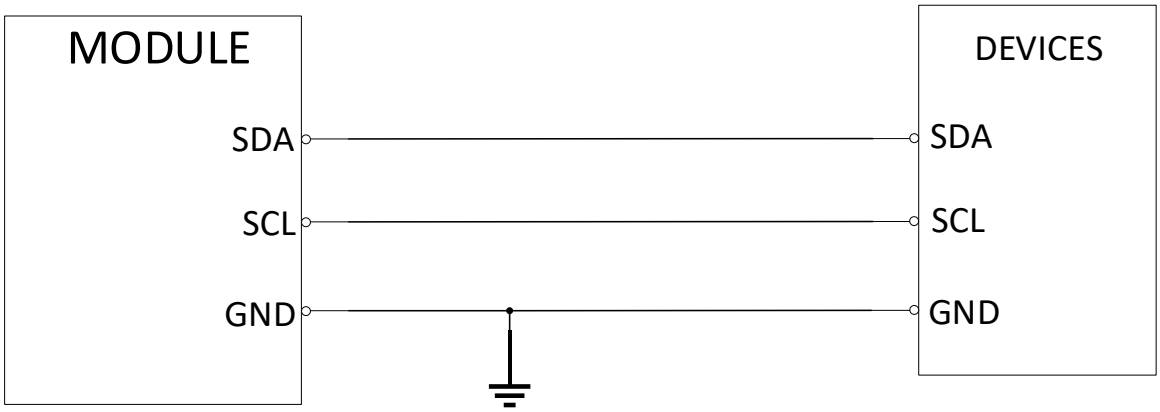


Figure 26 I2C design reference circuit

Note: 1. Special software versions are required to support access to I2C.

2. L508 I2C only supports the HOST mode.

4.11 Network light

4.11.1 Pin Description

Table 23 NETLIGHT

Pin No.	Pin Name	I / O type	Functional description
51	NETLIGHT	DO	Network indicator switch control

4.11.2 Interface application

The L508 module has a pin to control the LED display and can be used as an indicator of network connection status. A status light indicates that different patterns of flashing indicate different network states. The pin uses a GPIO, with an external NPN transistor and an External VBAT to drive the LED directly. Drive current capability varies depending on the external NPN type. DTC143ZEBTL is recommended with a maximum drive current of 100 ma， Figure 4-22 is a reference circuit diagram. The state of the indicator light can be designed and controlled by the host computer through instructions.

Table 24 NETLIGHT status

Net Status	Module working status
Always on	Searching Network/Call Connect
200ms ON, 200ms OFF	Data Transmit
800ms ON, 800ms OFF	Registered network
OFF	Power off / Sleep

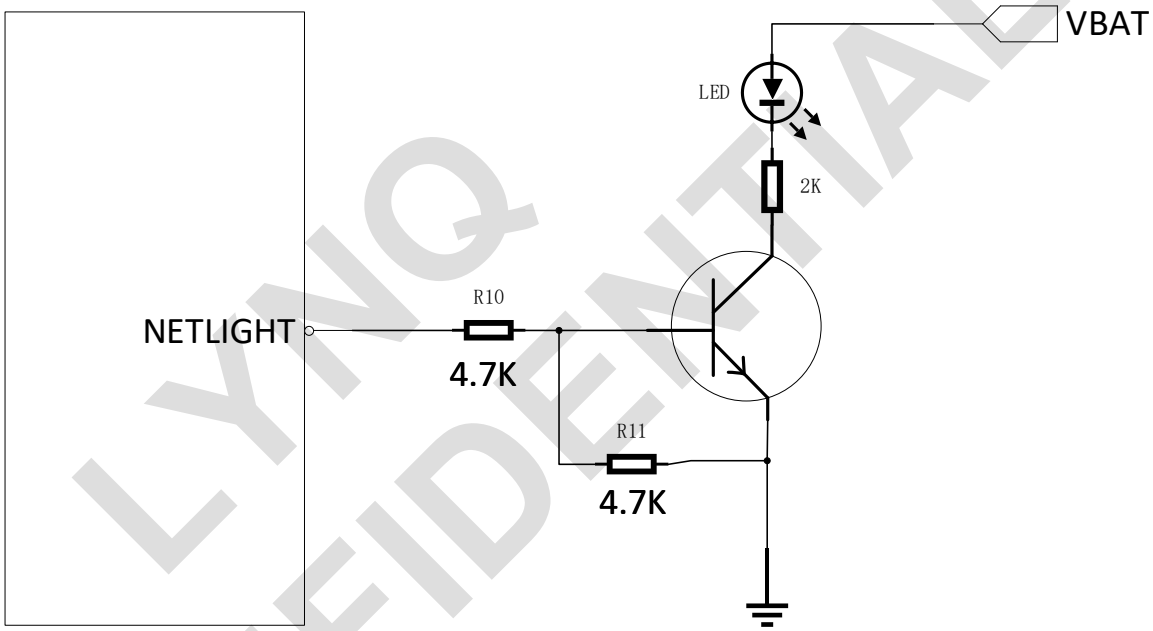


Figure 27 NETLIGHT reference circuit

4.12 System Status Indication

STATUS Pin is the status indicator PIN, when the STATUS is high, that the system boot is normal, when the STATUS is low, that the system abnormal or the system has been shut down.

Table 25 STATUS

Pin No.	Pin Name	I / O type	Functional description
49	STATUS	DO	System Status Display

4.13 Flight Mode

The FLIGHTMODE pin can be used to control the module to enter or exit flight mode. In flight mode, the internal RF circuitry of the L508 is turned off (this feature requires special software support). When the FLIGHTMODE PIN is low, the system goes into flight mode.

Table 26 FLIGHTMODE

Pin No.	Pin Name	I / O type	Functional description
54	FLIGHTMODE	DI	Flight Mode Control Terminal

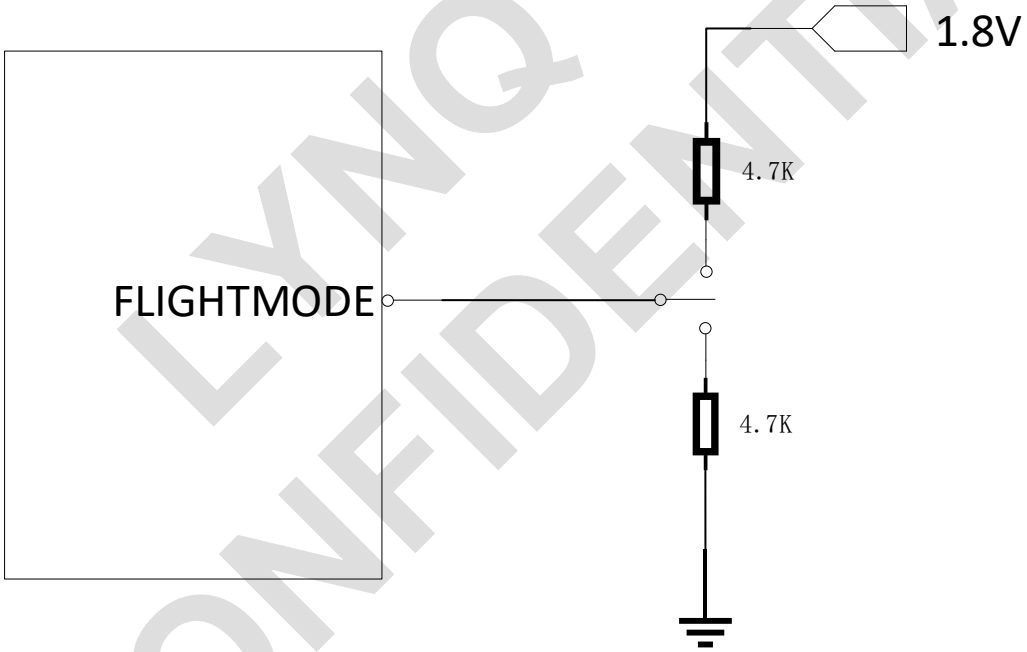


Figure 28 FLIGHTMODE design schematic

4.14 Forced USB download interface

4.14.1 Pin Description

The L508 can be configured to enter forced USB download mode by pulling up 85 PIN.

Table 27 Forced download interface definitions

Pin No.	Pin Name	I / O type	Functional description
85	DL_KEY	DI	Connect DL_KEY to VDD1V8 before boot on, then the system will enter USB forced download mode

4.14.2 Forced USB download interface application

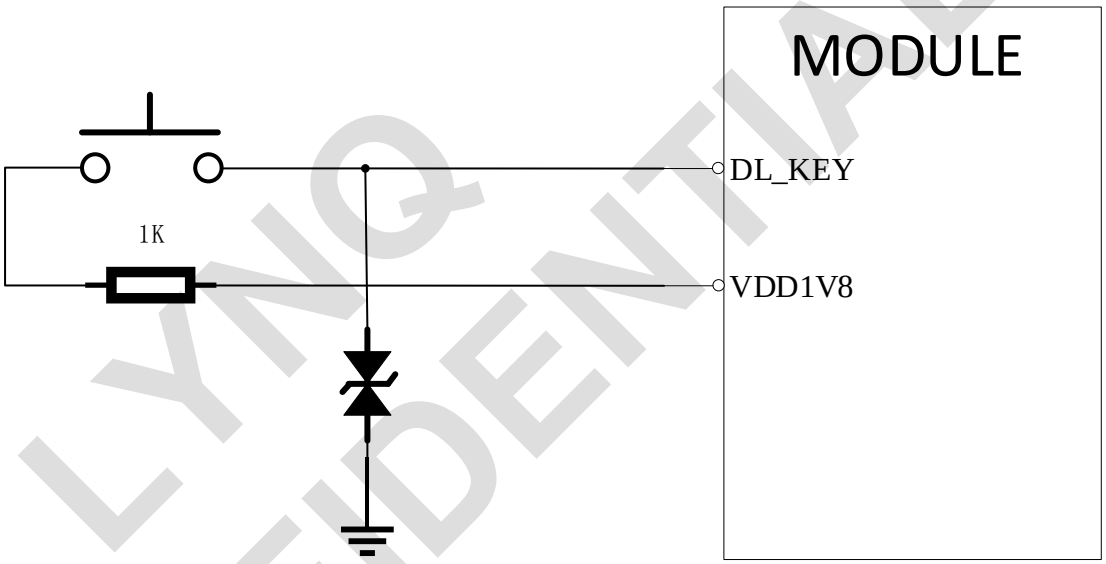


Figure 29 L508 download reference circuit

4.15 SD card interface

4.15.1 Pin Description

The module supports SD card with 4-bit data interface, or devices based on SDIO protocol. SD interface level can be adjusted at 1.8/3.0V.

Table 28 SD card interface definitions

Pin No.	Pin Name	I / O type	Functional description

21	MMC_CMD	DO	Secure digital controller 1 command
22	MMC_DATA0	B	Secure digital controller 1 data bit 0
23	MMC_DATA1	B	Secure digital controller 1 data bit 1
24	MMC_DATA2	B	Secure digital controller 1 data bit 2
25	MMC_DATA3	B	Secure digital controller 1 data bit 3
26	MMC_CLK	DO	Secure digital controller 1 clock
44	SD_LDO	PO	LDO output for SD card power, default voltage is 3.0V
48	MMC_CD	DI	Secure digital card detection

4.15.2 SD card reference design

CMD, CLK, DATA0, DATA1, DATA2 and DATA3 are all high-speed signal lines. During PCB design, these signals need to be controlled by 50ohm impedance, and do not cross with other routes. The routes should be placed in the inner layer as far as possible. CLK, CMD, DATA0, DATA1, DATA2, DATA3 line equal length processing; CLK needs to be packaged separately.

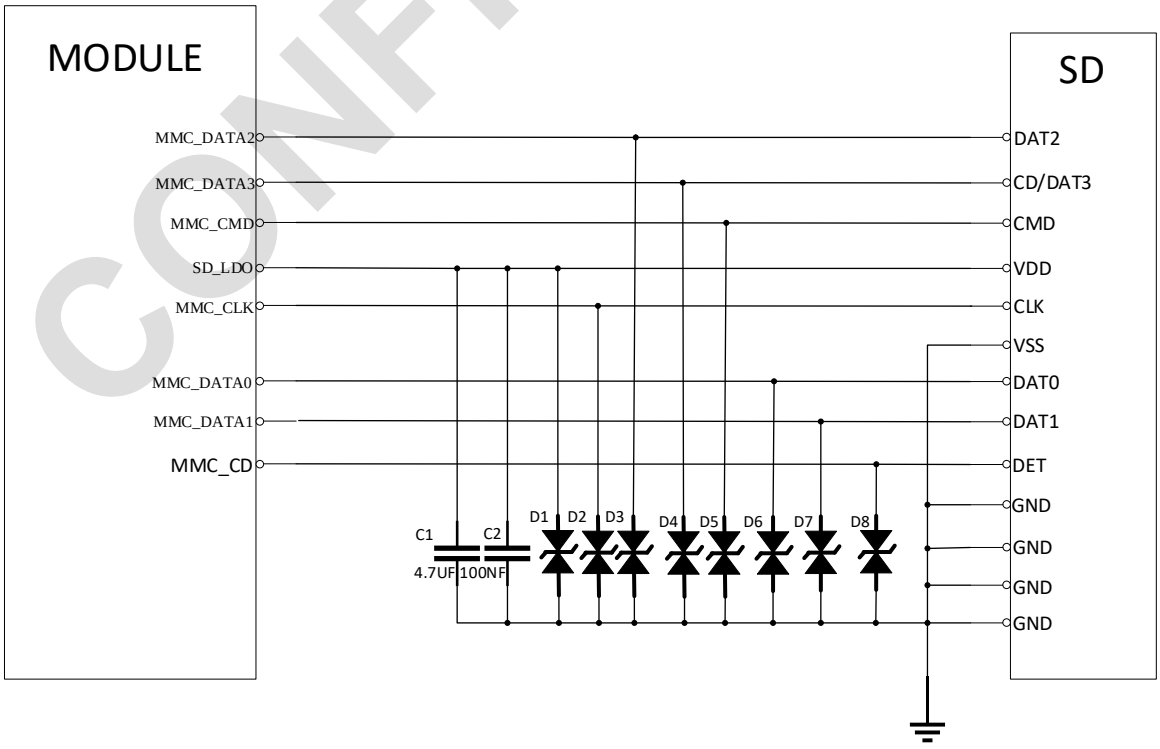


Figure 30 SD card reference design

4.16 SDIO_WIFI/EMMC interface

The L508 module provides a set of SDIO2.0/3.0 interfaces to the WIFI/EMMC chip, the interface level of SDIO is only 1.8V.

4.16.1 Pin Description

Table 29 SDIO_WIFI/EMMC interface definitions

Pin No.	Pin Name	I / O type	Functional description
15、34	VDD1V8	PO	LDO for 1/O
30	WLAN_PDN	DO	WLAN chip enable
			RST_n，use to reset EMMC chip
42	WLAN_DCDC_EN	DO	WLAN/EMMC external power enable
113	WIFI_CLK_26M	AO	26M clock output
116	WLAN_CLK_REQ	DI	WLAN clock request
117	WLAN_DAT1	B_PU	Secure digital controller 2 data bit 1
118	WLAN_DAT2	B_PU	Secure digital controller 2 data bit 2
119	WLAN_CMD	DO	Secure digital controller 2command
120	WLAN_DAT3	B_PU	Secure digital controller 2 data bit 3
121	WLAN_DAT0	B_PU	Secure digital controller 2 data bit 0
122	WLAN_CLK	DO	Secure digital controller 2 clock
123	WLAN_WAKE_HOST	DI	WLAN interrupt wake up module

4.16.2 SDIO reference design

CMD, CLK, DATA0, DATA1, DATA2 and DATA3 are all high-speed signal lines. During PCB design, these signals need to be controlled by 50ohm impedance, and do not cross with other routes. The

routes should be placed in the inner layer as far as possible. CLK, CMD, DATA0, DATA1, DATA2, DATA3 line equal length processing; CLK needs to be packaged separately.

Table 30 SDIO routing length inside the module

The length of routes outside the module should be considered the length of routes in the module. and the total length of routes should be equal.

Pin No.	Pin Name	Length (mm)
L508E		
117	WLAN_DAT1	14.81
118	WLAN_DAT2	25.53
119	WLAN_CMD	23.87
120	WLAN_DAT3	15.08
121	WLAN_DAT0	12.31
122	WLAN_CLK	16.66
L508LA/L508C		
117	WLAN_DAT1	11.01
118	WLAN_DAT2	28.36
119	WLAN_CMD	21.25
120	WLAN_DAT3	20.76
121	WLAN_DAT0	15.65
122	WLAN_CLK	14.12
L508TLC		
117	WLAN_DAT1	10.78
118	WLAN_DAT2	21.39
119	WLAN_CMD	19.75

120	WLAN_DAT3	17.28
121	WLAN_DAT0	14.60
122	WLAN_CLK	12.82

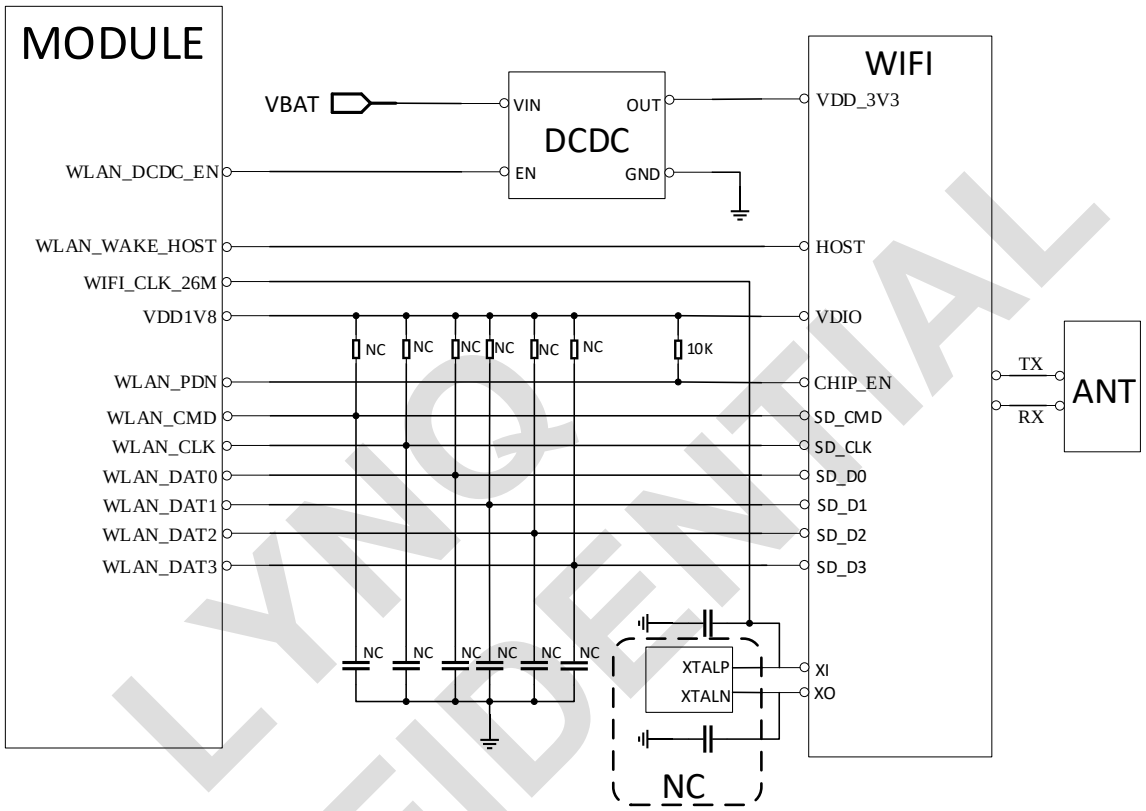


Figure 31 SDIO_WIFI reference design

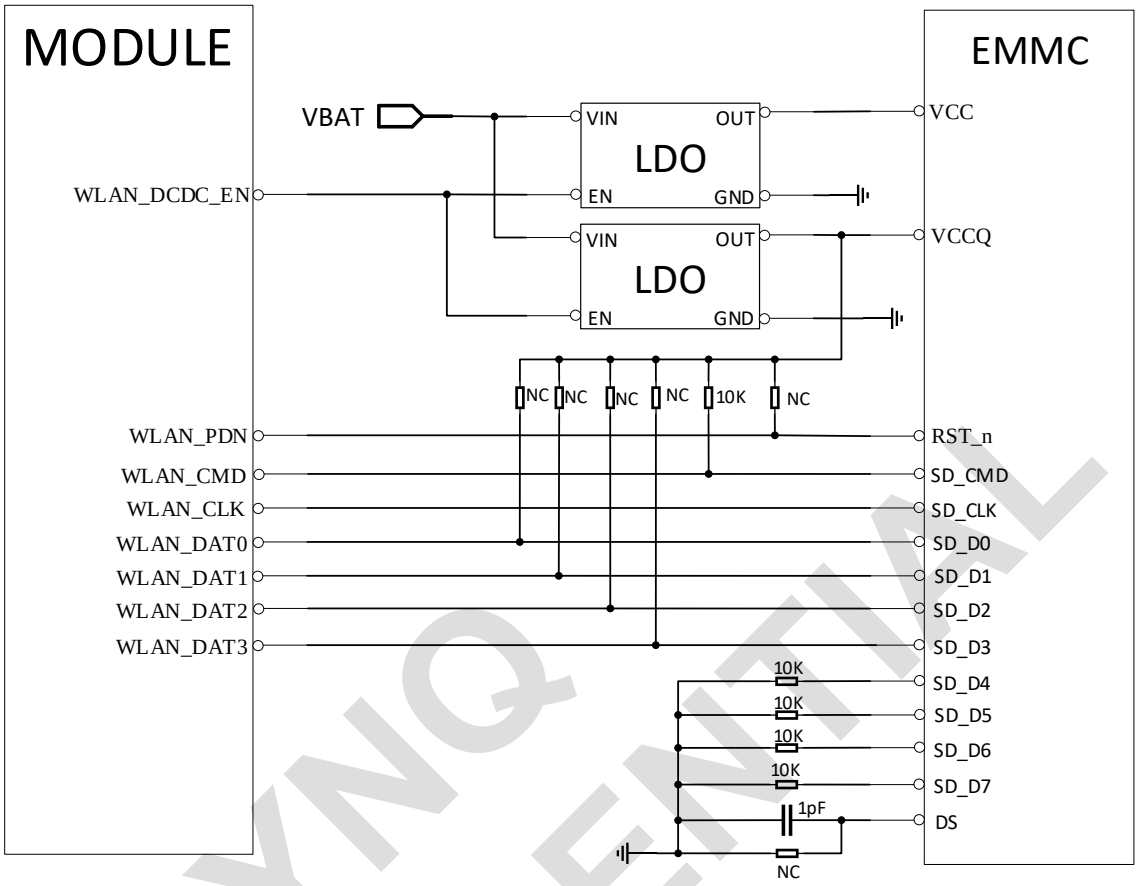


Figure 32 SDIO_EMMC reference design

4.17 PCIe interface

The L508 module provides a RC interface (PCIe Gen1 X1 Lane) to connect to WIFI chips or other peripherals. PCIe Gen1 has a maximum transmission speed of 2.5Gbps.

4.17.1 Pin Description

Table 31 PCIe interface definitions

Pin No.	Pin Name	I / O type	Functional description
70	UART_DCD	DO	PCIE_CHIP_EN，WIFI Chip cold start signal
119	WLAN_CMD	B_PU	PCIE_WK_IN，WIFI Wake-up module signal
122	WLAN_CLK	B_PU	PCIE_RSTN，WIFI Chip hot start signal

124	PCIE_TXP	AO	Differential transmit data signal positive
125	PCIE_TXN	AO	Differential transmit data signal negative
126	PCIE_RXP	AI	Differential receive data signal positive
127	PCIE_RXN	AI	Differential receive data signal negative
128	PCIE_REFCLK_P	AO	Reference clock signal positive
129	PCIE_REFCLK_N	AO	Reference clock signal negative

4.17.2 PCIe reference design

PCIE needs differential routing, data and clock routing impedance difference of 100ohm, equal length control within 3mm, good isolation protection

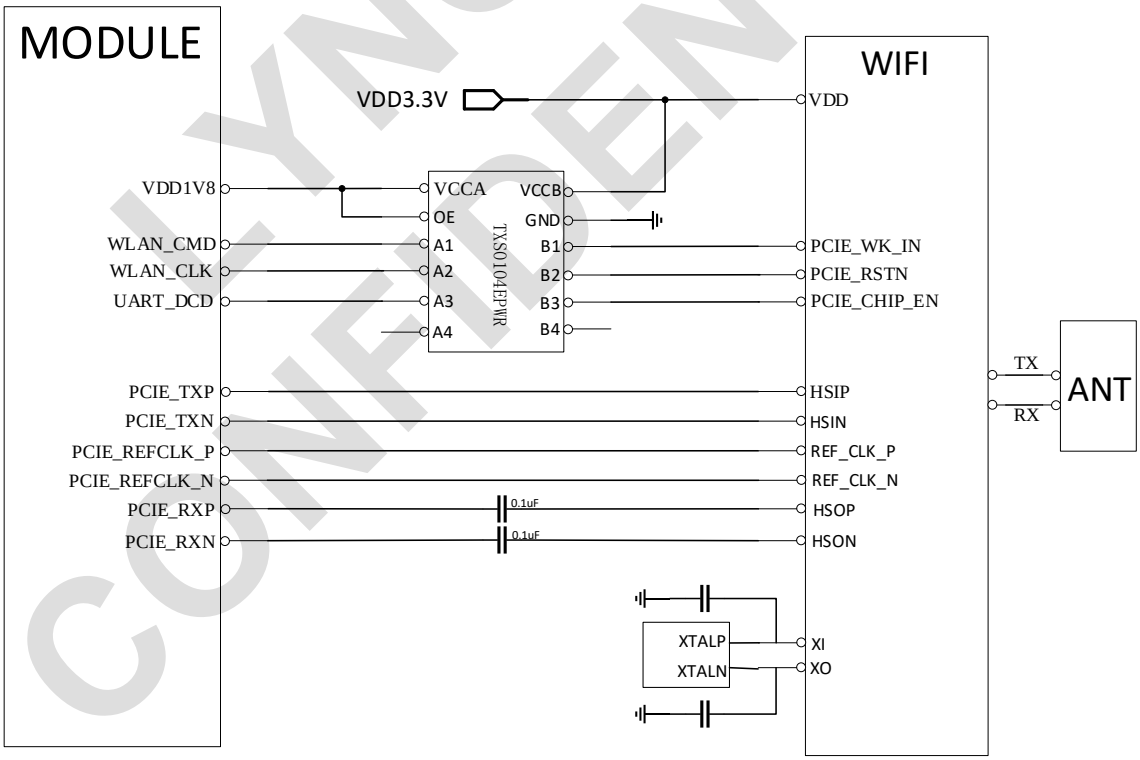


Figure 33 PCIe reference design

4.18 RMII/RGMII interface

L508 module supports 10M/100M Ethernet RMII interface, 1000M RGMII interface, the RMII interface level is determined by 108 PIN RMII_LDO, RMII_LDO input power is 1.8V/3.3V adjustable.

4.18.1 Pin Description

Table 32 RMII/RGMII interface definitions

Pin No.	Pin Name	I / O type	Functional description
66	GPIO_20	DO	RMII_RST, low effective, Ethernet chip reset signal
100	RMII_RX_CTRL	B_PU	Collision and Data Valid
101	RMII_RXD0	B_PU	Receive Data 0
102	RMII_RXD1	B_PU	Receive Data 1
30	WLAN_PDN	B_PU	Receive Data 2
84	GPIO_05	B_PU	Receive Data 3
103	RMII_CLK	B_PU	Reference clock
104	RMII_TXD0	B_PU	Transmit data 0
105	RMII_TXD1	B_PU	Transmit data 1
49	STATUS	B_PD	Transmit data 2
51	NETLIGHT	B_PD	Transmit data 3
50	WAKEUP_IN	B_PU	Transmit Clock
106	RMII_TX_CTRL	B_PD	Transmit enable
107	RMII_INT	B_PU	RMII interrupt output
108	RMII_LDO	PI	RMII power input (1.8/3.3V)
109	RMII_MDC	B_PD	Management clock
110	RMII_MDIO	B_PU	Management data I/O

4.18.2 RMII/RGMII reference design

The receiving and sending of data signals of RMII/RGMII requires a single-ended impedance of 50 ohm, and the equal length should be controlled within 3mm. Isolation measures should be taken.

Table 33 RMII routing length inside the module

The length of routes outside the module should be considered the length of routes in the module. and the total length of routes should be equal.

Pin No.	Pin Name	Length (mm)
L508E		
101	RMII_RXD0	11.43
102	RMII_RXD1	17.82
30	WLAN_PDN（RGMII_RXD2）	33.57
84	GPIO_05（RGMII_RXD3）	24.92
103	RMII_CLK	13.17
100	RMII_RX_CTRL	12.48
104	RMII_TXD0	13.39
105	RMII_TXD1	14.85
49	STATUS（RGMII_TXD2）	43.16
51	NETLIGHT（RGMII_TXD3）	39.76
50	WAKEUP_IN（RGMII_TXCLK）	42.68
106	RMII_TX_CTRL	16.16
L508LA/L508C		
101	RMII_RXD0	6.64
102	RMII_RXD1	14.48
30	WLAN_PDN（RGMII_RXD2）	32.45
84	GPIO_05（RGMII_RXD3）	24.37

103	RMII_CLK	9.70
100	RMII_RX_CTRL	11.38
104	RMII_TXD0	8.65
105	RMII_TXD1	11.66
49	STATUS（RGMII_TXD2）	42.53
51	NETLIGHT（RGMII_TXD3）	41.03
50	WAKEUP_IN（RGMII_TXCLK）	42.13
106	RMII_TX_CTRL	17.37
L508TLC		
101	RMII_RXD0	9.90
102	RMII_RXD1	10.36
30	WLAN_PDN（RGMII_RXD2）	32.75
84	GPIO_05（RGMII_RXD3）	23.98
103	RMII_CLK	13.81
100	RMII_RX_CTRL	7.18
104	RMII_TXD0	10.84
105	RMII_TXD1	13.24
49	STATUS（RGMII_TXD2）	41.37
51	NETLIGHT（RGMII_TXD3）	41.01
50	WAKEUP_IN（RGMII_TXCLK）	42.04
106	RMII_TX_CTRL	10.67

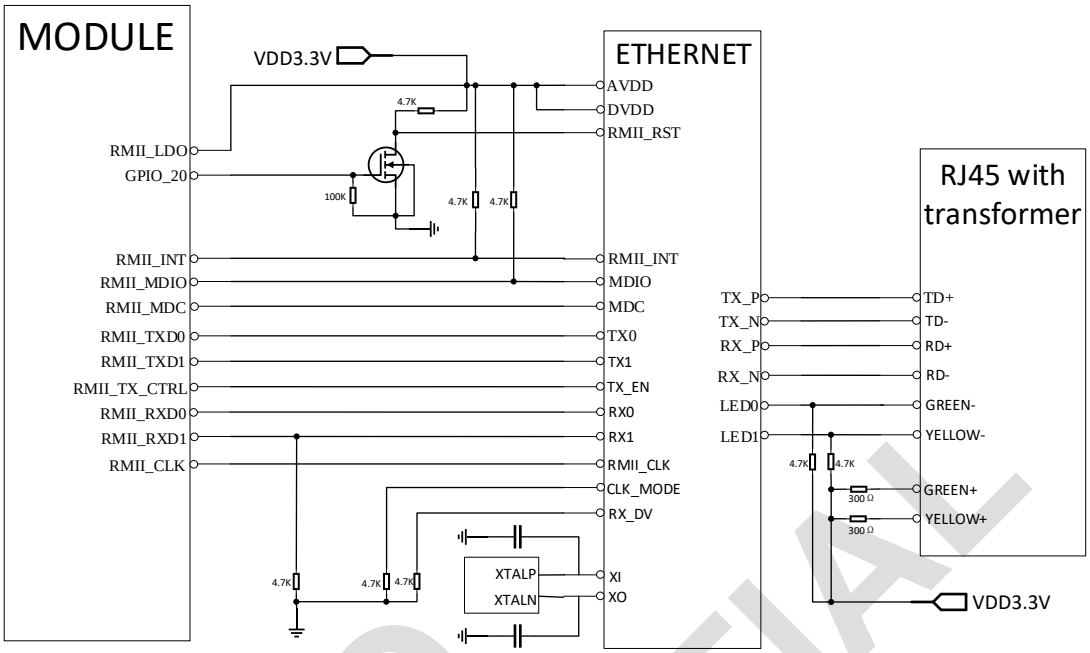


Figure 34 RMII Ethernet reference design

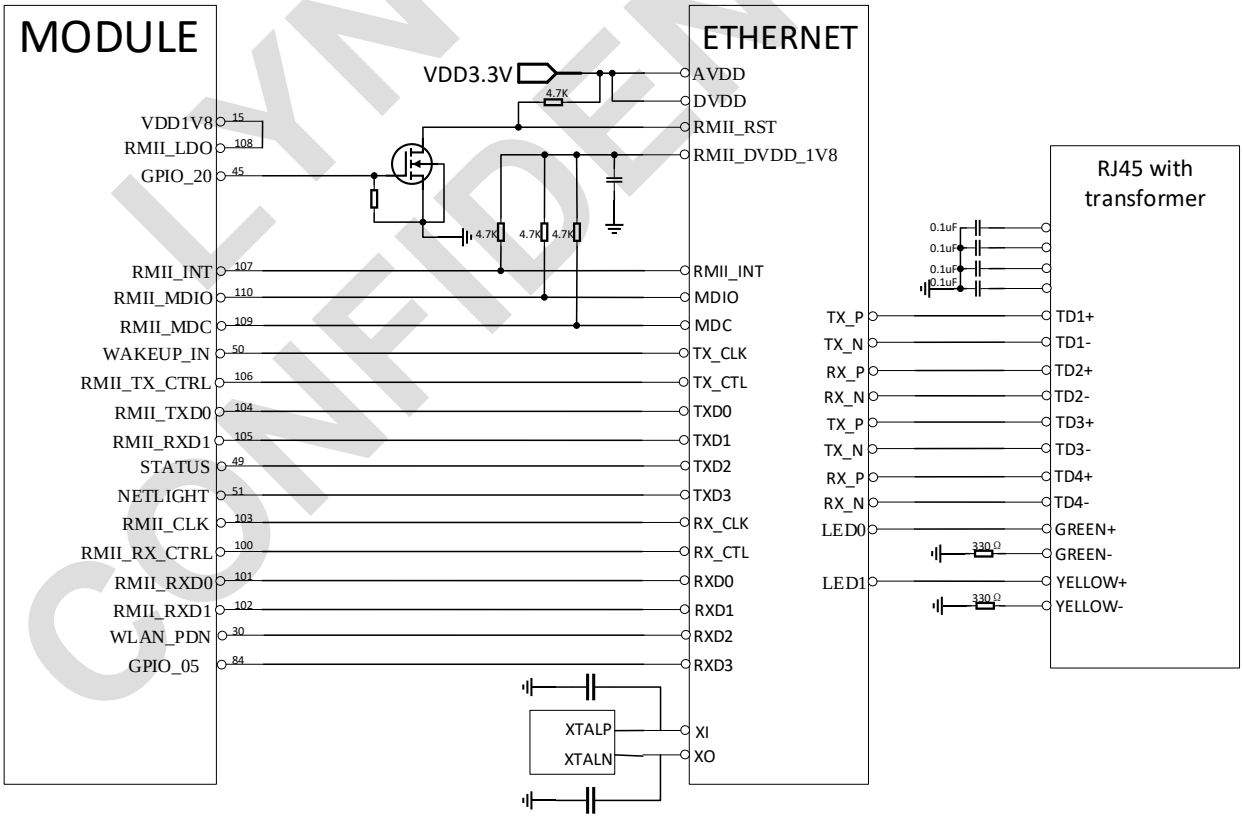


Figure 35 RMII Ethernet reference design

4.19 AUDIO interface

L508 module provides one analog audio input channel and one analog output channel. The output channel is (Class-AB): THD<-85dB@32-ohm loading

4.19.1 Pin Description

Table 34 AUDIO interface definitions

Pin No.	Pin Name	I / O type	Functional description
27	MICN	AI	Microphone negative input
29	MICP	AI	Microphone1 positive input
31	RECN	AO	Receiver negative output
32	RECP	AO	Receiver positive output

4.19.2 AUDIO reference design

The MIC channel has been biased up inside the module. MIC and REC should carry out differential wiring and do a good job of isolation and protection.

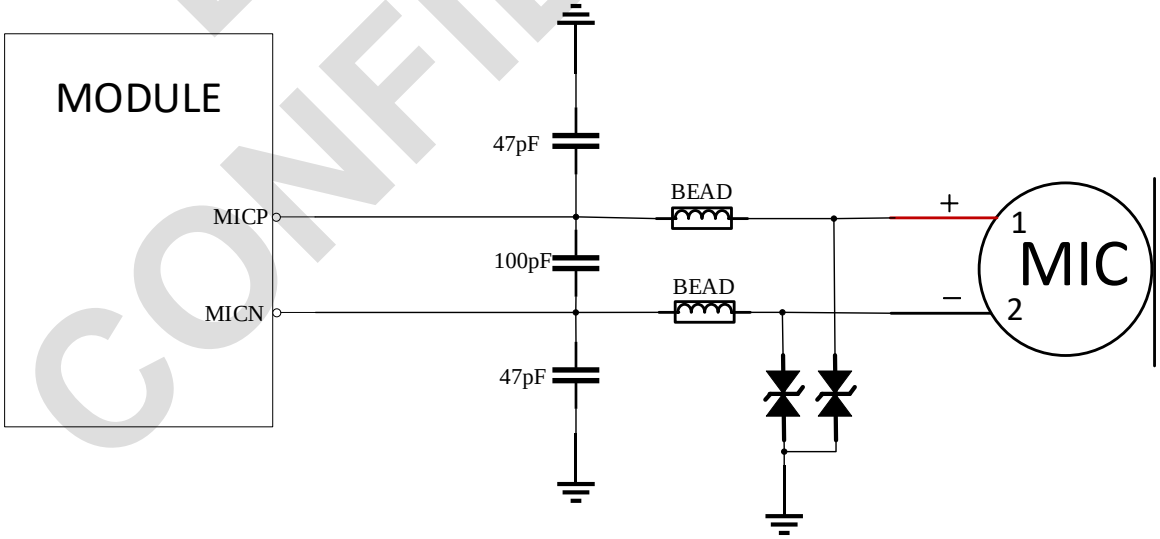


Figure 36 Electret microphone reference design

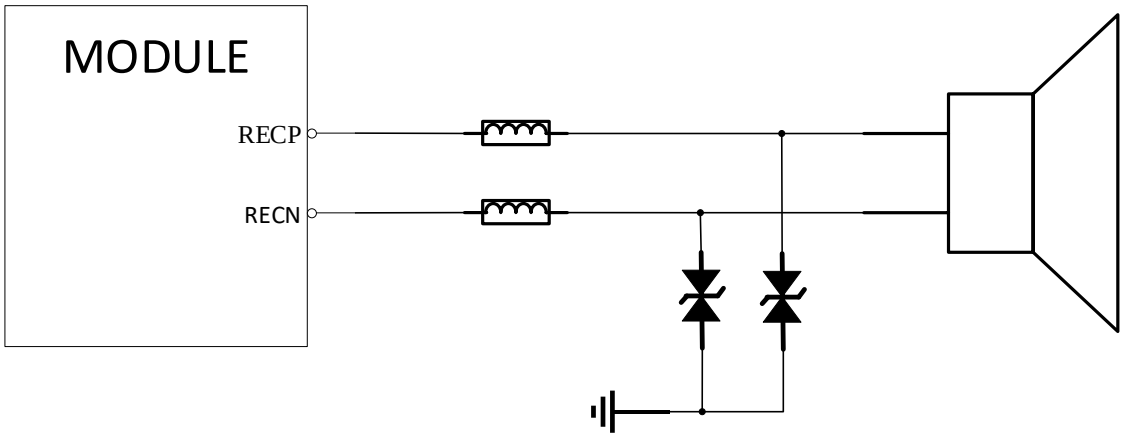


Figure 37 Receiver reference design

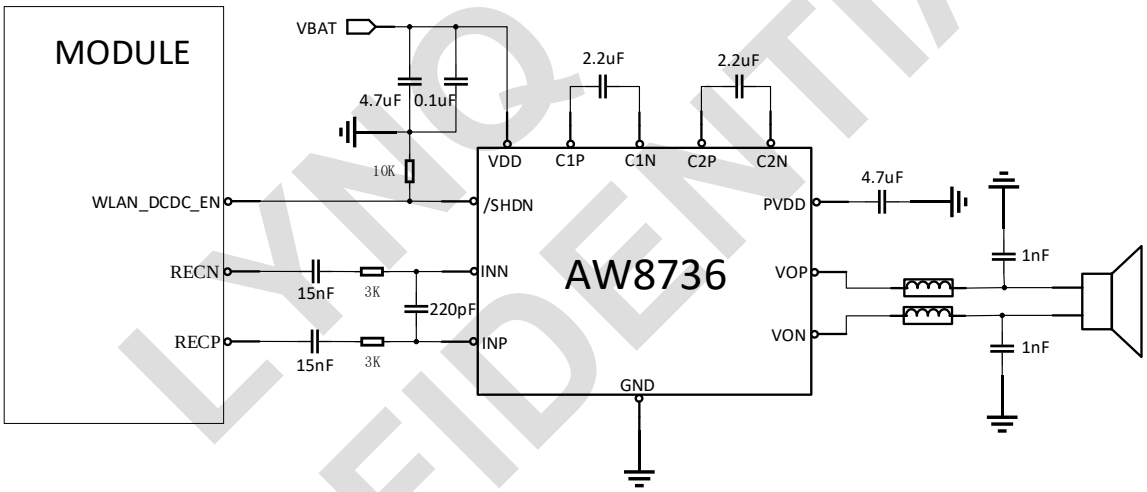


Figure 38 External class K amplifier reference design

4.20 ADC

Pin Description as follows:

Table 35 ADC

Pin No.	Pin Name	I / O type	Description
46	ADC2	AI	L508E/L508TLC: Voltage detection range:0-1.3V
47	ADC1	AI	

			L508LA/L508C: Voltage detection range:0-1.8V. Accuracy is affected by temperature, can be used when the requirements are not high

4.21 GPIOs

The L508 has a rich GPIO interfaces and pins defined as follows:

Table 36 GPIO list

Pin No.	Pin Name	GPIO	voltage	Reset state	Wakeup
6	SPI_CLK	GPIO_33	1.8V	B-PD	▲
7	SPI_MISO	GPIO_35	1.8V	B-PD	▲
8	SPI_MOSI	GPIO_36	1.8V	B-PD	▲
9	SPI_CS	GPIO_34	1.8V	B-PD	▲
28	GPIO_21	GPIO_21	1.8V	B-PU	▲
30	WLAN_PDN	GPIO_04	1.8V	B-PU	▲
42	WLAN_DCDC_EN	GPIO_123	1.8V	B-PD	▲
49	STATUS	GPIO_13	1.8V	B-PU	▲
50	WAKEUP_IN	GPIO_12	1.8V	B-PU	▲
51	NETLIGHT	GPIO_14	1.8V	B-PD	▲
52	WAKEUP_OUT	GPIO_118	1.8V	B-PU	▲
54	FLIGHTMODE	GPIO_120	1.8V	B-PU	▲
55	I2C_SCL	GPIO_49	1.8V	B-PU	▲
56	I2C_SDA	GPIO_50	1.8V	B-PU	▲
66	UART_RTS	GPIO_32	1.8V	B-PU	▲
67	UART_CTS	GPIO_31	1.8V	B-PU	▲

68	UART_RX	GPIO_51	1.8V	B-PU	▲
69	UART_RI	GPIO_23	1.8V	B-PU	▲
70	UART_DCD	GPIO_24	1.8V	B-PU	▲
71	UART_TX	GPIO_52	1.8V	B-PU	▲
72	UART_DTR	GPIO_22	1.8V	B-PU	▲
73	PCM_OUT	GPIO_27	1.8V	B-PD	▲
74	PCM_IN	GPIO_28	1.8V	B-PD	▲
75	PCM_SYNC	GPIO_26	1.8V	B-PD	▲
76	PCM_CLK	GPIO_25	1.8V	B-PD	▲
100	RMII_RX_CTRL	GPIO_00	RMII_LDO	B-PU	▲
101	RMII_RXD0	GPIO_01	RMII_LDO	B-PU	▲
102	RMII_RXD1	GPIO_02	RMII_LDO	B-PU	▲
103	RMII_CLK	GPIO_03	RMII_LDO	B-PU	▲
104	RMII_TXD0	GPIO_06	RMII_LDO	B-PU	▲
105	RMII_TXD1	GPIO_07	RMII_LDO	B-PU	▲
106	RMII_TX_CTRL	GPIO_15	RMII_LDO	B-PD	▲
107	RMII_INT	GPIO_18	RMII_LDO	B-PU	▲
109	RMII_MDC	GPIO_16	RMII_LDO	B-PD	▲
110	RMII_MDIO	GPIO_17	RMII_LDO	B-PU	▲
112	LCD_BK_EN	GPIO_126	1.8V	B-PD	▲
114	UART2_TX	GPIO_53	1.8V	B-PU	▲
115	UART2_RX	GPIO_54	1.8V	B-PU	▲
116	WLAN_CLK_REQ	GPIO_125	1.8V	B-PD	▲
123	WLAN_WAKE_HOST	GPIO_117	1.8V	B-PU	▲

Note: *The GPIO level of 100, 101, 102, 103, 104, 105, 106, 107, 109 and 110 pins is determined by 108PIN RMII_LDO, which supports both 1.8V and 3.3V voltages.*

4.22 Power on/off and reset interface

4.22.1 Pin Description

When the VBAT is in normal state(3.2<VBAT<4.6), the Module will be powered on by the following two ways:

- Pulling the PWRKEY low more than 0.5s, then release
- Pulling the EXTON1N low

Any of the above events will trigger system power on.

There are two ways to reset the module. Pulling the PWRKEY long time, will reboot the PMIC, PMIC powered on will reboot the CPU;

- Pulling the PWRKEY long time, will reboot the PMIC, PMIC powered on will reboot the CPU
- Pulling the RESET, will reboot the CPU

Interface definitions are shown in the following table:

Table 37 boot and reset key interface definitions

Pin No.	Pin Name	I / O type	Functional description
3	EXTON1N	AI	Power-on trigger, level trigger (active low)
4	RESET	DI	reset input. Active low
86	PWRKEY	AI	Input pad generally connected to a keypad power-on Button. Active low

Note: The pull-up voltage of PWRKEY and EXTON1N was consistent with that of VBAT, and the pull-up voltage of RESET was 1.8V.

4.22.2 Power-on sequence

VBAT power, VAON (RTC clock source), PWRKEY also synchronous power. After the PWRKEY pin is lowered, the module starts up, and all internal power sources such as VDD1V8 start up one after another. When the Status pin becomes high, it means the module starts up and can be used normally.

Table 38 power-on sequencing

Symbols	Pin Name	Min	Typ	Max	Unit
Ton	Start-up low level pulse width	0.5		16	s
TSTATUS	BOOT time (based on the Status Pin)	12	13	--	s
TUART	BOOT time (according to UART judgement)	11	12	--	s
VIH	PWRKEY pin input high level voltage	0.7*VBAT	--	VBAT	V
VIL	PWRKEY pin input low level voltage	0	--	0.3*VBAT	V

The boot sequence is shown below

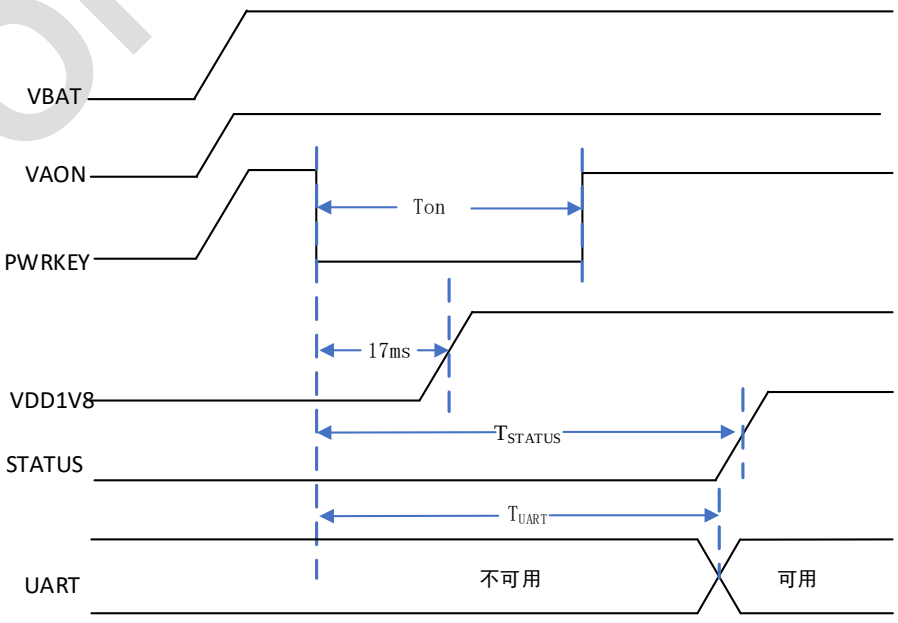


Figure 39 Power on sequence diagram

Note: the STATUS Pin is an indication of the module's running Status, and a high signal indicates that the module is finished booting and initializing the process, otherwise the PIN is low

4.22.3 Power-off sequence

Modules have the following shutdown methods:

- Shut down using the PWRKEY Pin
- Shutdown using the "AT CPOF" command

Note: 1. For a detailed description of "AT + CPOF" , refer to documentation [1] .

2. Overvoltage (high or low) may also cause the module to shut down automatically.

3. Exceeding the limit temperature of the module may also cause the module to shut down automatically.

Table 39 Power-off sequencing

Symbols	Pin Name	Min	Typ	Max	Unit
TOFF	Power off low level pulse width	16	--	--	s
TSTATUS	Shutdown time (judged by the Status Pin)	25	26	--	s
TUART	BOOT time (according to UART judgement)	14	15	--	s

Users can power off by pulling down the PWRKEY signal. The shutdown sequence is shown in the following figure:

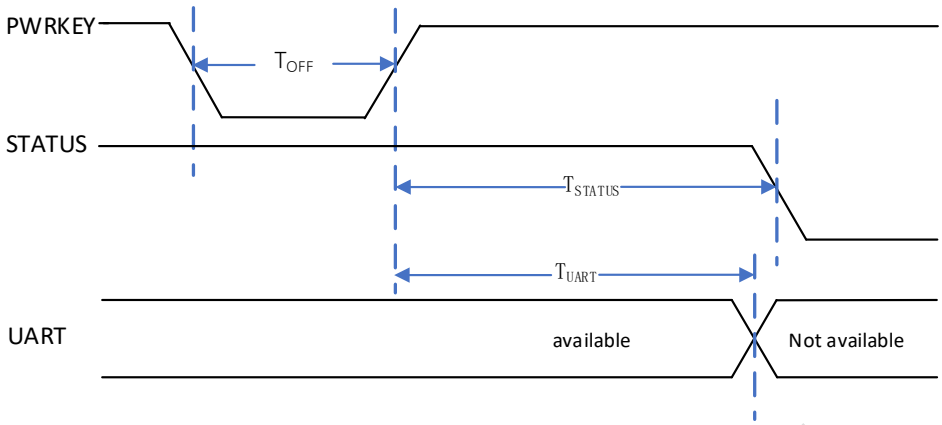


Figure 40 Power-off sequence diagram

Note: the Status Pin can be used to determine whether the power is on, and when the module is powered up and initialized, the STATUS output is high, otherwise it remains low.

4.22.4 Reset sequence

L508 can reset the module by pulling down the RESET or PWRKEY pin. Refer to 4.22.1 for a description of restarting the module.

Table 40 electrical properties of reset key signals

Symbols	Pin Name	Min	Typ	Max	Unit
VIH	Reset pin input high level voltage	1.26	1.8	2.0	V
VIL	Reset pin input low level voltage	-0.3	0	0.54	V

Note: It is recommended to use the RESET pin only in emergency situations, such as when the module is not responding. In addition, the RESET pin is not valid when the module is turned off.

4.22.5 Interface application

PWRKEY, EXTON1N and RESET circuit can refer to the following diagram of the design circuit.

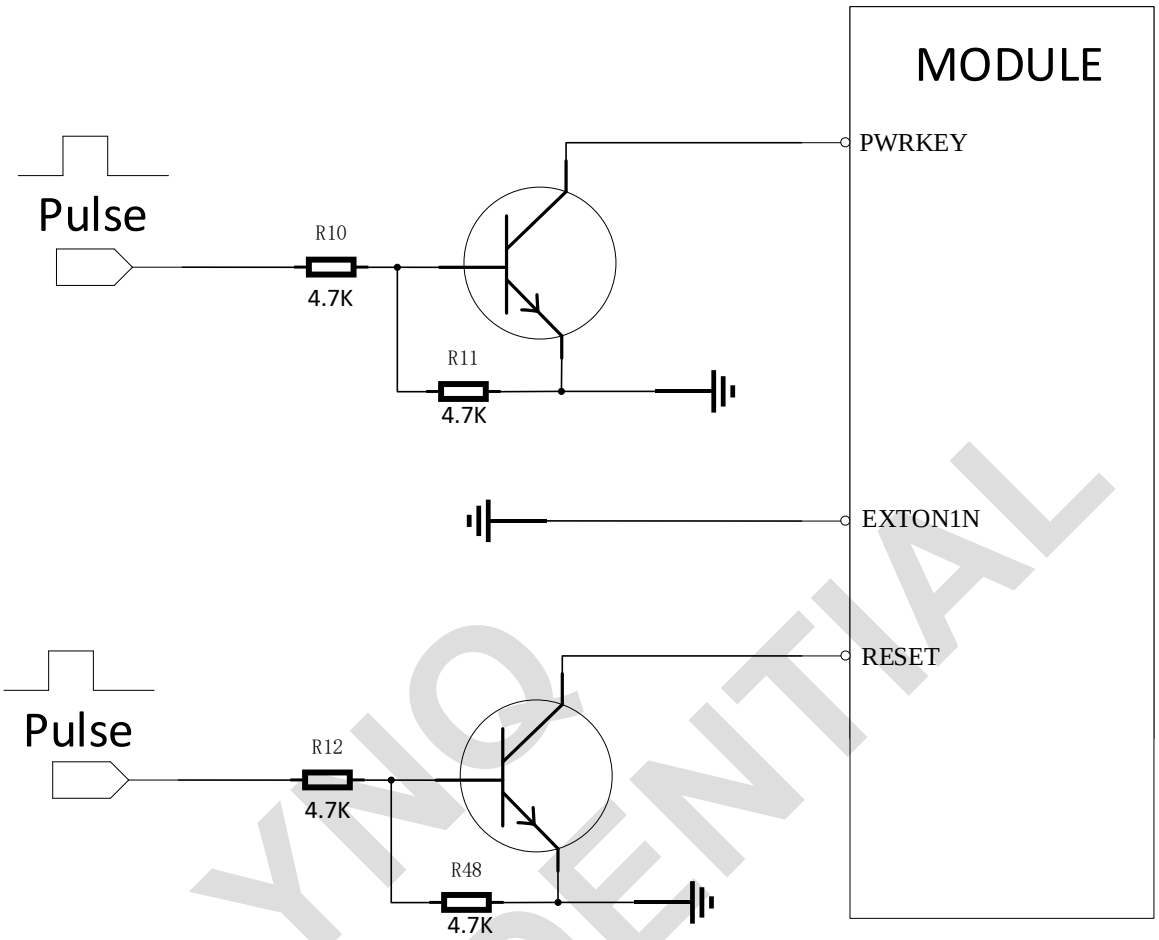


Figure 41 PWRKEY/RESET/EXTON1N reference circuit

Another way to control the PWRKEY, RESET, EXTON1N pin, is to use a physical key switch directly.

Place a TVS near the button for ESD protection. The following is the reference circuit:

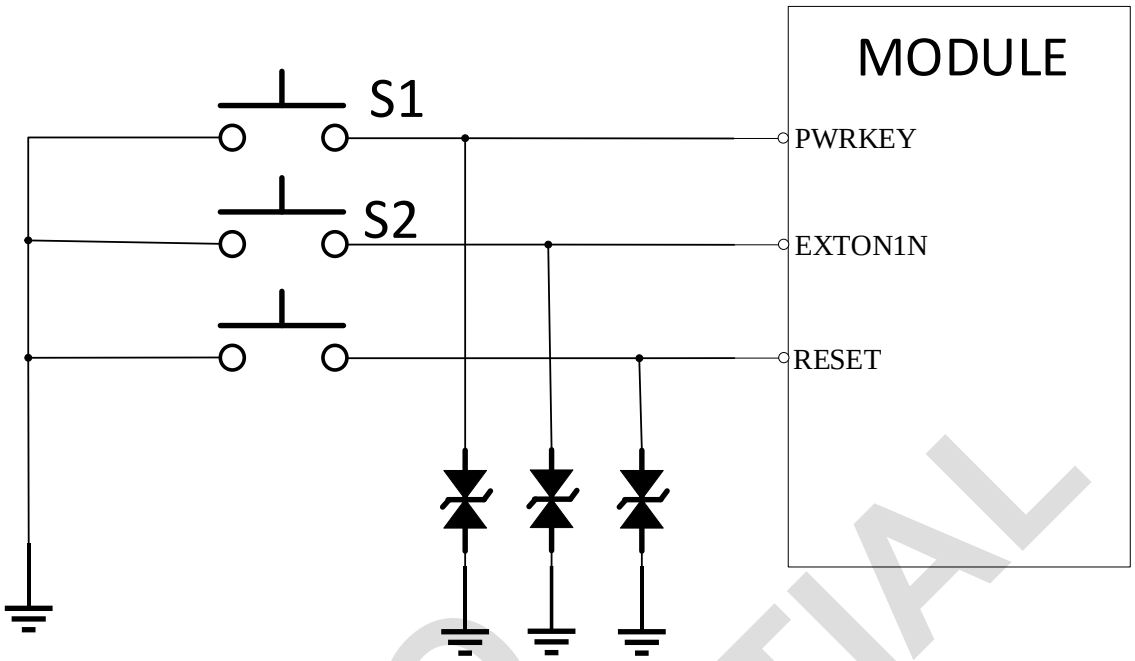


Figure 42 PWRKEY/RESET reference circuit

4.23 Antenna interface

4.23.1 RF signal PCB layout guide

The L508 module provides the RF antenna interface on the LCC pad. The antenna signal line can be matched through a microstrip line or other type of RF line via an antenna matching T or type circuit. The impedance must be controlled at 50 Ω。

It is recommended that the insertion loss between the antenna feed point and the antenna should meet the following requirements:

- GSM900<0.5dB
- DCS1800 <0.9dB
- WCDMA 2100<0.9dB
- WCDMA 900<0.5 dB
- CDMA BC0<0.5 dB
- TDSCDMA 1900/2000<0.9dB
- LTE (F<1GHz) <0.5dB

- LTE (1GHz<F<2GHz) <0.9dB
- LTE (2GHz<F) <1.2dB

The antenna feed point definition is shown in the following table:

Table 41 antenna interface definitions

Pin No.	Pin Name	I / O type	Functional description
59	ANT_DRX	AI	Diversity antenna
79	GNSS_ANT	AI	GPS antenna
82	ANT_MAIN	AI，AO	Main antenna

4.23.2 Interface application

To facilitate antenna tuning and authentication testing, RF connectors and antenna matching circuits should be added. The following are recommended circuits:

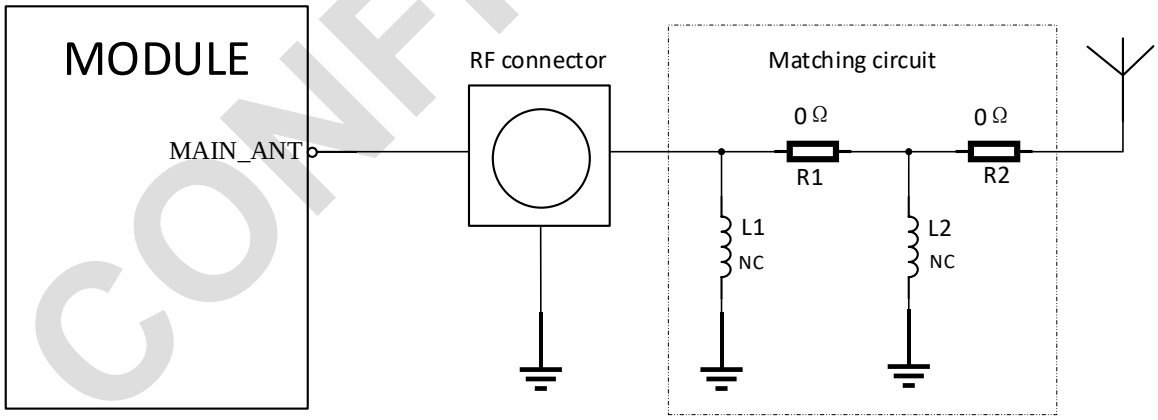


Figure 43 Main antenna matching circuit schematic

In figure, components R1, L1, L2, and R2 are used for antenna matching, and the value of the components depends on the antenna being debugged. By default, R1, R2 are 0 ohms resistors, and L1, L2 are reserved for debugging. The RF connectors shown in this figure are used for RF

performance testing and should be placed close to the module's antenna pins. Line impedance between components must be controlled at 50 ohms.

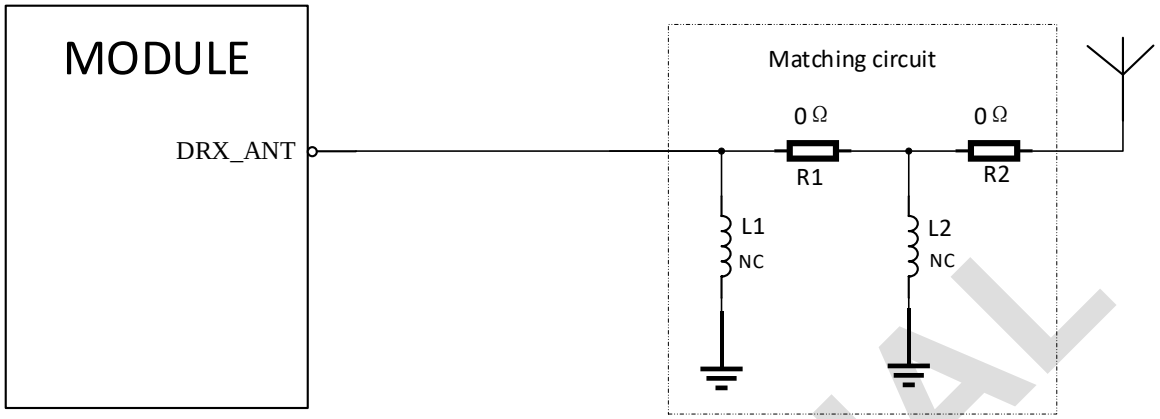


Figure 44 DRX antenna matching circuit schematic

In the image above, R1 and R2, L1 and L2 are used for diversity antenna matching. By default, R1, R2 are 0 resistors, and L1, l2 are reserved for debugging.

Note: LTE Diversity Antennas are recommended to be retained for modules supporting diversity reception, as there are many high-frequency TDD-LTE designs such as Band38, band40 and Band41. Because of the high insertion loss of RF LINES, the receiving sensitivity of these bands will be greatly affected if there is no diversity antenna.

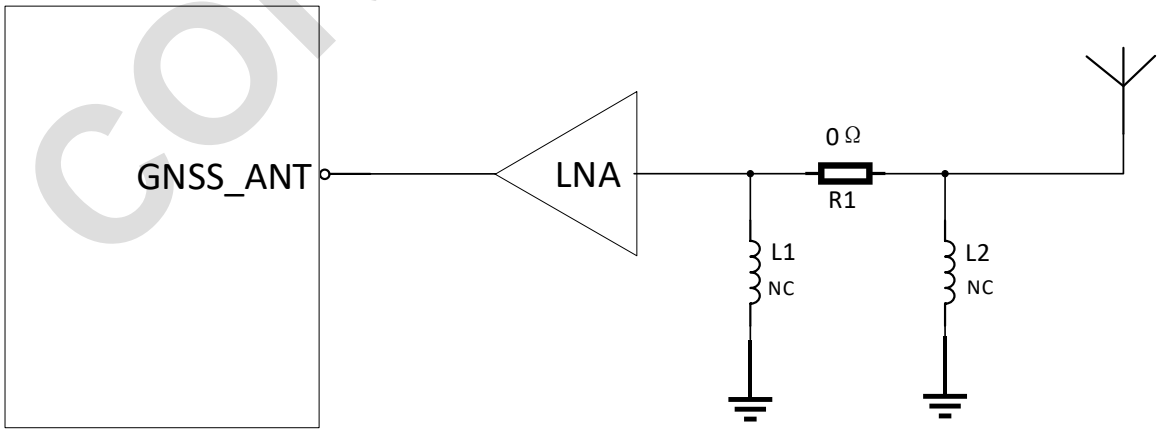


Figure 45 GNSS antenna matching circuit schematic

In the image above, elements R1, L1, and L2 are used for antenna matching, and the value of the elements depends on the antenna being debugged.

In figure 43, the user can add an external LNA for better gain.

The L508LA/L508C/L508TLC integrated GNSS (GPS/BEIDOU/GLONASS) satellite and network information provides a high availability solution that provides industry-leading performance and accuracy.

Key indicators for GNSS ARE AS FOLLOWS:

- Tracking sensitivity: -160 dBm
- Capture sensitivity : -155dBm
- Cold start sensitivity: -147 dBm
- CN value: C/N0 = S - (-130dBm: 41dB) S= Input Signal Intensity
- Accuracy (open space): 2.5m (CEP50)
- First Positioning (open space): Hot Start <1s Cold start 35s
- Receiving type: 64-channel, C/A Code
- GPS, L1 frequency: (1575.42±1.023MHz),
- Beidou frequency: 1559.05 ～1563.14 MHz
- GLONASS: 1597.5~1605.8 MHz
- Default update rate: 1 Hz
- GNSS DATA format: NMEA-0183

4.23.3 Antenna Layout guideline

In layout design, the antenna RF transmission line must have a characteristic impedance of 50 ohms, which is determined by the substrate, the width of the line and the distance from the ground plane. Figure below shows the reference clearance area for the antenna feed point in the layout.

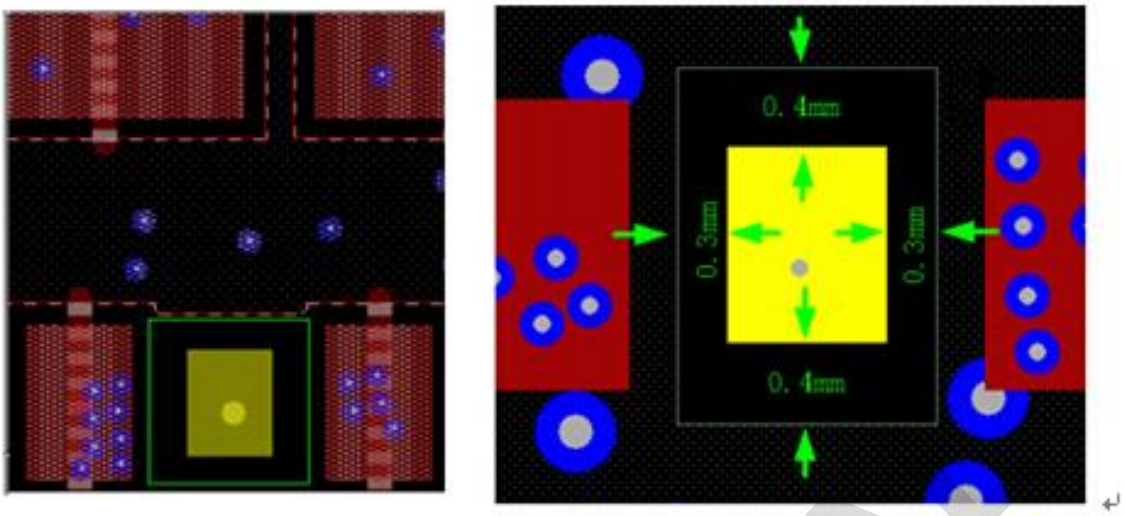


Figure 46 antenna feed point

5 Product characteristics

5.1 Absolute maximum ratings

Operating the L508 under conditions beyond its absolute maximum ratings (Table 43) may damage the device.

Table 42 absolute parameters

Parameters	Min	Max	Unit
VBAT limit voltage	-0.5	6.0	V
USB limit voltage	-0.5	5.8	V
I/O limit voltage: GPIO, I2C, PCM, UART, SD1_DET, USIM_DET	-0.3	2.1	V
I/O limit voltage: USIM	-0.3	3.3	V

5.2 Operating conditions

5.2.1 Operating conditions

Table 43 Normal working voltage of module

Parameters	Minimum value	Typical value	Maximum value	Unit
VBAT Voltage	3.2	3.8	4.6	V
USB_VBUS Voltage	3.5	5.0	5.5	V

5.2.2 Work mode

The following table describes the definition of the L508 work pattern.

Table 44 working mode

Patterns		Definition
Normal operating mode	(GSM/WCDMA /TD-SCDMA/EVDO/LTE)Sleep	In this case, the current consumption of module will bereduced to the minimal level. In sleep mode, the module can still receive paging message and SMS.
	(GSM/WCDMA /TD-SCDMA/EVDO/LTE) Idle	Software is active. Module is registered to the GSM/WCDMA/TD-SCDMA/EVDO/LTE network, andthe module is ready to communicate.
	(GSM/WCDMA /TD-SCDMA/EVDO) taking	Connection between two subscribers is in progress. In thiscase, the power consumption depends on network settings such as DTX off/on, FR/EFR/HR, hopping sequences, antenna.
	(GPRS/EDGE/WCDMA/TD -SCDMA/EVDO/LTE) Standby	Module is ready forGPRS/EDGE/WCDMA/TD-SCDMA/EVDO/LTE data transfer, but no data is currently sent or received. Inthis case, power consumption depends on network settings and EDGE/HSPA+ /LTE configuration.
	(GPRS/EDGE/WCDMA/TD -SCDMA/EVDO/LTE) Data transfer	There isGPRS/EDGE/WCDMA/TD-SCDMA/EVDO/LTE data transfer in progress. In this case, power consumptionis related to network settings (e.g. power control level); uplink/downlink data rates and GPRS configuration (e.g. used multi-slot settings).
Minimum mode		AT command “AT+CFUN” can be used to set the module to a minimum functionality mode without

	removing the power supply. In this mode, the RF part of the module will not work or the USIM card will not be accessible, orboth RF part and USIM card will be closed, and the serial port is still accessible. The power consumption in this mode is lower than normal mode.
Power off	Through the "AT + CPOF" command or lower PWRKEY pin can power off L508. At this mode, the module of internal power supply will be closed, and the system is stop running also. The UART and USB are unavailable.
Sleep mode	In sleep mode, the module power consumption to a minimum, but the module is still able to receive paging information and SMS.

5.2.3 Current consumption (TBD)

Table 45 VBAT consumption current (VBAT = 3.8V)

Power off	
Power off current	20uA
GSM Sleep/Idle	
GSM/GPRS supply current （GNSS off，without USB）	Sleep mode @ BS_PA_MFRMS=2 Typical: Idle mode @ BS_PA_MFRMS=2 Typical：
UMTS sleep/idle	
WCDMA current （GNSS off，without USB）	Sleep mode @DRX=9 typical： Idle mode @DRX=9 typical：
TD-SCDMA current （GNSS off，without USB）	Sleep modetypical： Idle modetypical：

EVDO current （GNSS off，without USB）	Sleep modetypical： Idle mode typical：
LTE Sleep/Idle	
LTE supply current （GNSS off，without USB）	Sleep mode typical： Idle mode typical：TBD
GSM Talking	
GSM 900	@Power level #5 typical：
DCS1800	@Power level #0 typical：
UMTS Talking	
WCDMA B1	@power 24dBm typical：
WCDMA B2	@power 24dBm typical：
WCDMA B5	@power 24dBm typical：
WCDMA B8	@power 24dBm typical：
TD-SCDMA 1900	@power 24dBm typical：
TD-SCDMA 2000	@power 24dBm typical：
CDMA BC0	@power 24dBm typical：
GPRS Data transmission	
GSM 900 (1RX,4 TX)	@power level #5 typical：
DCS1800 (1RX,4 TX)	@power level #0 typical：
GSM 900 (3RX, 2TX)	@power level #5 typical：
DCS1800 (3RX, 2TX)	@power level #0typical：
EDGE Data transmission	
GSM 900	@power level #8typical：

(1RX,4 TX)	
DCS1800 (1RX,4 TX)	@power level #2typical：
GSM 900 (3RX, 2TX)	@power level #8typical：
DCS1800 (3RX, 2TX)	@power level #2typical：
HSDPA Data transmission	
WCDMA B1	@power 24dBm typical：
WCDMA B2	@power 24dBm typical：
WCDMA B5	@power 24dBm typical：
WCDMA B8	@power 24dBm typical：
TD-SCDMA Data transmission	
TDSCDMA 1900	@power 24dBm typical：
TDSCDMA 2000	@power 24dBm typical：
EVDO Data transmission	
BC0	@power 24dBm typical：
LTE Data transmission	
LTE-FDD B1	@5Mbps typical： @10Mbps typical： @20Mbps typical：
LTE-FDD B2	@5Mbps typical： @10Mbps typical： @20Mbps typical：
LTE-FDD B3	@5Mbps typical： @10Mbps typical： @20Mbps typical：

LTE-FDD B4	@5Mbps typical： @10Mbps typical： @20Mbps typical：
LTE-FDD B5	@5Mbps typical： @10Mbps typical：
LTE-FDD B7	@5Mbps typical： @10Mbps typical： @20Mbps typical：
LTE-FDD B8	5Mbps typical： @10Mbps typical：
LTE-FDD B12	@5Mbps typical： @10Mbps typical：
LTE-FDD B13	@5Mbps typical： @10Mbps typical：
LTE-FDD B17	@5Mbps typical： @10Mbps typical：
LTE-FDD B20	typical：
LTE-TDD B38	@5Mbps typical： @10Mbps typical： @15Mbps typical：
LTE-TDD B39	@5Mbps typical： @10Mbps typical： @15Mbps typical：
LTE-TDD B40	@5Mbps typical： @10Mbps typical： @15Mbps typical：
LTE-TDD B41	@5Mbps typical： @10Mbps typical：

	@15Mbps typical：

5.3 Working and storage temperature

The working storage temperature of this product is shown in Table 47.

Table 46 Operating temperature

Parameters	Min	Typ	Max	Unit
Normal operation temperature	-40	25	85	℃
Storage temperature	-45	25	90	℃

Note: when the operating temperature exceeds the operating temperature of the module, some of the RF performance of the module may deteriorate, and may cause shutdown, restart and other faults.

5.4 Electrostatic protection

L508 is electrostatic sensitive device, therefore, the user in the production, assembly and operation of the module must pay attention to the electrostatic protection. L506 ESD performance parameters in the following table:

Table 47 ESD performance parameters (temperature: 25 °C, humidity: 45%)

Pin	Contact discharge	Air Discharge
VBAT GND	±5KV	±10KV
Other PADS	±0.5KV	±1KV

6 Design Guideline

This chapter provides the general design guidance of the product, users can refer to the design guidance for design, so that the product to achieve better performance.

6.1 General Design rules and requirements

When designing the peripheral circuit of this product, the user must first ensure that the external power supply circuit can provide sufficient power supply capacity and control the differential impedance of 90 ohm ± 10% for the high-speed signal line USB. For the general signal interface, users are required to design strictly in accordance with our requirements, in line with the interface signal level matching, in case of inconsistent level damage module. The product has good RF performance, customers need to design the side antenna circuit and do the corresponding impedance control, otherwise it will affect the RF performance of the whole machine.

6.2 Circuit reference design

It is required that the power supply capacity of VBAT on the board side of the system should be more than 2A to meet the peak current demand of the module, and the mean current of the power supply on the system side should be more than 0.9 a. The power supply line on the board side of the system should have enough line width and form a good return current with the ground plane. In addition, the 100-micrometer energy storage capacitor should be added in the design of the power supply circuit to ensure the instantaneous power supply, and the power supply ripple should be controlled within 100 MV, detailed functional modules see the corresponding functional description, the overall reference circuit details see "L508 Design" .

6.3 RF circuit design

6.3.1 Matters needing attention in the initial stage of antenna design

- Pre-project evaluation

The selection of the antenna position first ensures that the antenna and the base station remain in the Horizontal Direction, which produces the highest efficiency; second, try to avoid placing in the switching power supply or data lines, chips and other devices that may produce electromagnetic interference or near the chip. At the same time, avoid positions where the hand can be placed on the antenna, which prevents the human body from attenuating the antenna, and take into account both the reduced radiation and the structural feasibility. Therefore, the layout evaluation needs to be done by the structure, ID, circuit, and antenna engineers at the beginning of the design.

- Antenna matching circuit

Antenna placement for notebook products: The ideal placement of LCD in the upper left or upper right, this location is far from the motherboard, the electromagnetic interference is small, and considering the relatively far from the human body, the SAR index is easy to meet; The next best position is the left or right side of the LCD. Other products such as routers, e-books and so on according to the specific characteristics of the product evaluation.

- Antenna footprint recommendation

Because different antenna manufacturers may use different antenna forms, therefore, the antenna reserve space is also different: 4G 7-mode 17-frequency main antenna: 8mm (thick) * 12mm (wide) * 100mm (long).

- Motherboard Layout

There is a strong interference in the area of the motherboard, and the experimental results show that the performance of the module will be worse if the module is placed in the area. When designing a laptop, it is best to separate the module from the MOTHERBOARD PCB rather than install it on the motherboard. If the separation is not possible, the module should be as far away from the chip and memory, power interface, data line interface and other modules and devices that may cause EMI.

- Main antenna matching circuit

If the connection between the RF port of the module and the antenna interface is required, the microstrip or stripline between the module RF test stand and the antenna interface RF test stand is designed for 50 ohms of characteristic impedance in the circuit design of the motherboard, if the RF connector of the antenna can be directly stuck on the RF test stand of the module, the connection between the RF port of the module and the antenna interface can be omitted.

6.4 EMC AND ESD design recommendations

The user should take the EMC problem caused by the Signal integrity and power integrity into account when designing the whole machine. When the layout of the peripheral circuit of the module is laid out, the power and signal lines should be laid out with the width of 2 times of the spacing between the lines, it can effectively reduce the coupling between signals, so that the signals have a "clean" return path. When designing the peripheral power circuit, the decoupling capacitor should be placed close to the module power pin, the high-frequency high-speed circuit and the sensitive circuit should be far away from the PCB edge, and the layout should be isolated as far as possible to reduce the mutual interference, the sensitive signal is protected and the shielding design is made for the circuit or device which may interfere with the operation of the module.

This product is embedded in the side of the system board, need to pay attention to the design of ESD protection, key input and output signal interface, such as U Sim Card Signal Interface, need to place ESD devices nearby for protection, in addition to the side of the motherboard, the user is required to design the structure parts and PCB layout reasonably, ensure the metal shield shell to be grounded sufficiently, and set up a smooth discharge channel for electrostatic discharge.

6.5 Product Recommendation Upgrade Program

L508 updates firmware via USB by default, so it is recommended that USB test points or interfaces be set aside at design time to facilitate firmware updates for subsequent products.

7 Storage, Production and Package

7.1 Storage

The rank of moisture proof of the module is level 3. There is an obvious sign on the table of the internal and the external packaging.

In the vacuum sealed bag, the module can be stored for 12 months when the temperature is below 40°C and the humidity is below 90% under good air circulation.

Humidity level is described detail as follows:

Table 48 Humidity Level

Rank	Factory Environment 23±5°C, Relative Humidity < 60%RH
1	No control < 30°C / 85%RH
2	One year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Baking before using, SMT during the time table signs

Notes: Moving, storage, production of module must meet the demand of IPC/JEDEC J-STD-033.

7.2 Production

The module is a humidity sensitive device. If the device needs reflow soldering, disassembly and maintenance, we must strictly comply with the requirements of humidity sensitive device. If module is damp, a reflow soldering or using a hot-air gun maintenance will lead to internal damage, because the water vapor has the rapid expansion of the burst, causing physical injury to the device, like PCB foaming and BGA component fail. So customers should refer to the following recommendations.

7.2.1 Module confirmation and moisture

The module in the production and packaging process should be strictly accordance with the humidity sensitive device operation. The factory packaging is vacuum bag, desiccant, and humidity indicator card. Please pay attention to the moisture control before SMT and the confirmation of the following aspects.

Demand of Baking confirmation

Smart module uses vacuum sealed bag, which can make it stored for 12 months under the condition of temp 40°C and humidity < 90%. The module should be baked before reflowing soldering if any of the conditions below happen.

1. Storage exceeds the time limit.

2. Package damages and vacuum bags have air leakage.

3. Humidity indicating card change the color at 10%.

4. Module is placed naked in the air over 168 hours.

5. Module is placed naked in the air under 168 hours but not temp 30°C and humidity < 60%.

Baking condition confirmation

The moisture proof level of the smart module is level 3. And the baking conditions are as follows.

Table 49 Baking Conditions

Baking conditions	**125±5°C / 5%RH**	**45±5°C / 5%RH**
Baking time	8 hours	192 hours
Description	Not use the original tray	Can use the original tray

Notes: The original anti-ESD tray temperature does not exceed 50°C. Otherwise the tray will be deformed.

The anti-ESD tray of the original packaging is only used for packaging, and can't be used as a SMT tray.

During taking and placing, please take notes of ESD and cannot be placed as overlay.

Customer product maintenance

If maintenance module after SMT, it is easy for damp module to damage when removing, so the module disassembly and other related maintenance operations should complete within 48 hours after SMT, or need to bake and then maintenance the module.

Because the module return from the field work can't ensure the dry state, it must be baked in accordance with the conditions of baking, then for disassembly and maintenance. If it has been exposed to the humid environment for a long time, please properly extend the baking time, such as 125°C/36 hours.

7.2.2 SMT reflow attentions

The module has the BGA chips, chip resistances and capacitances internally, which will melt at high temperature. If module melt completely encountered a large shock, such as excessive vibration of reflux conveyor belt or hit the board, internal components will easily shift or be false welding. So, using intelligent modules over the furnace need to pay attention to:

- Modules can't be vibrate larger, namely customer requirements as far as possible in orbit (chain) furnace, furnace, avoid on the barbed wire furnace, in order to ensure smooth furnace.

- The highest temperature can't too high. In the condition that meet the welding quality of customer motherboard and module, the lower furnace temperature and the shorter maximum temperature time, the better.

Some customer's temperature curve in the line is not suitable, high temperature is too high, and customer motherboard melt good, but non-performing rate is on the high side. Through the analysis of the causes, it found that melt again of BGA components lead device offset and short circuit. After adjusting the temperature curve, it can ensure that the customer's motherboard the welding quality, and also improve the pass through rate. Non-performing rate is controlled below the 2/10000.

7.2.3 SMT stencil design and the problem of less tin soldering

Part of customers found false welding or circuit short when reflowing. The main reason is module tin less, PCB distortion or tins too large. Suggestions are as follows:

- Suggest use ladder stencil, which means the depth of the region of module is thicker than other areas. Please adjust validation according to the measured thickness of solder paste, the actual company conditions and experience value. The products need to strictly test.

- Stencil: Reference module package and the user can adjust according to their company experience; Outside of the module, the stencil extends outside. The GND pads use the net stencil.

7.2.4 SMT attentions

If customer motherboard is thin and slender with a furnace deformation, warping risks, you will be suggested to create "a furnace vehicle" to ensure the welding quality. Other production proposals are as follows:

- The solder pastes use brands like Alfa.

- The module must use the SMT machine mount (important), and do not recommend manually placed or manual welding.

- For SMT quality, Please ensure the necessary condition according to actual condition of factory before SMT, like SMT pressure, speed (very important), stencil ways.

- We must use the reflow oven more than 8 temperature zones, and strictly control the furnace temperature curve.

  Recommended temperature:

  B. constant temperature zone: temperature 140-210°C, time: 60s-120s.

  E. recirculation zone: PEAK temperature 220-245°C, time: 45s-75s.

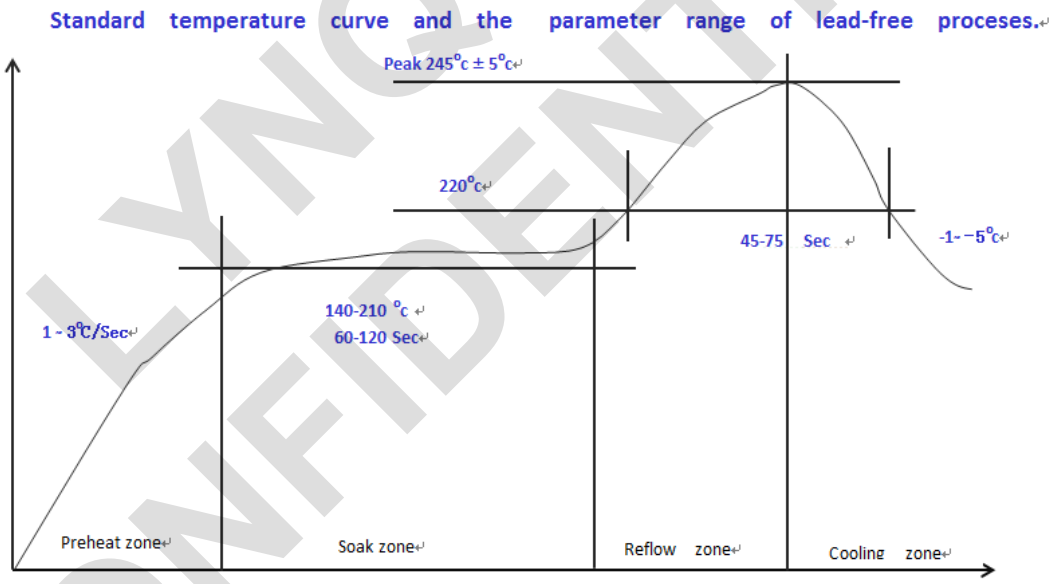


Figure 47 Temperature Curve

Notes: Customer's board deformation must be controlled well. By reducing the number of imposition or increasing patch clamp to reduce the deformation.

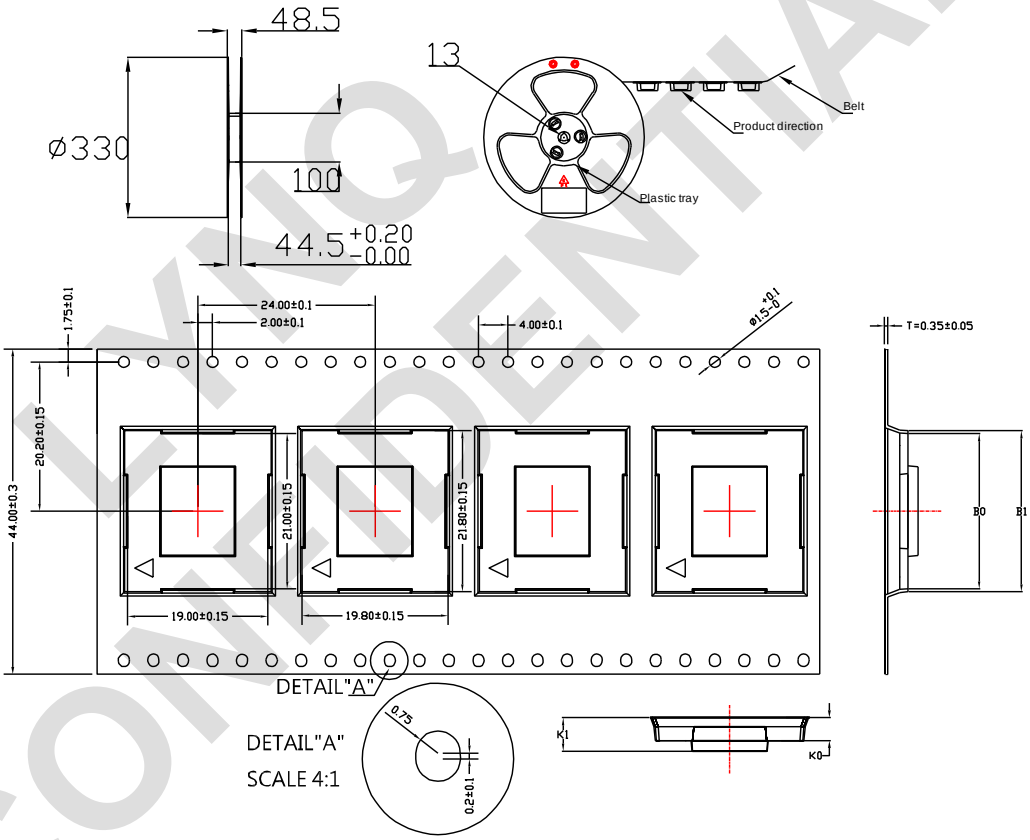
Module thickness of the stencil is recommended to be thickened, and the rest position can be maintained by 0.1mm.

7.3 Packaging Information

The L508 Series module are packaged with a roll of tape and sealed with a vacuum-sealed antistatic bag.

Coil tape

One coil can hold 500 modules, as shown in the figure.



ITEM	W	T	A0	A1	B0	B1	K0	K1	P	F	E	D	D1	P0	P2
DIM	44.0	0.35	19.0	19.8	21.0	21.8	3.2	4.5	24.0	20.2	1.75	1.5		4.0	2.0
TOLE	±0.3	±0.05	±0.15	±0.15	+0.15 −0.10	±0.15	±0.15	±0.15	±0.1	±0.15	±0.1	+0.10 −0.00	+0.10 −0.00	±0.1	±0.1

Figure 48 Coil Tape Information (Unit: mm)

8 Safety Information

For the reasonable usage of the module, please comply with all these safety notices of this page. The product manufacturers should send followed safety information to user, operator or product's spec.

The devices using the module may disturb some electronic equipment. Put the module away from the phone, TV, radio and automation equipment to avoid the module and the equipment to interfere with each other.

Shut down the mobile device or change to flying mode before boarding. The Using of wireless appliances in an aircraft is forbidden to avoid the interference, or else cause to unsafe flying, even violate the law.

In hospital or health care center, switch off the mobile devices. RF interference may damage the medical devices, like hearing-aid, cochlear implant and heart pacemaker etc.

Mobile devices can't guarantee to connect in all conditions, like no fee or with an invalid SIM card. When you need emergent help, please remember using emergency calls and make sure your device power on in an area with well signal.

Put the module away from inflammable gases. Switch off the mobile device when close to gas station, oil depot, chemical plant etc.

The module is not water proof. Please don’t use the module in the area with high humidity like bathroom, which will decelerate the physical performance, insulation resistance and mechanical strength.

Non-professionals can’t teardown the module which will damage it. Refer to the specification or communicate the related staffs to repair and maintain it.

Please switch on the module before cleaning. The staffs should be equipped with anti-ESD clothing and gloves.

The users and product manufacturers should abide by the national law of wireless modules and devices. If not, Mobiletek will not respond the related damages.