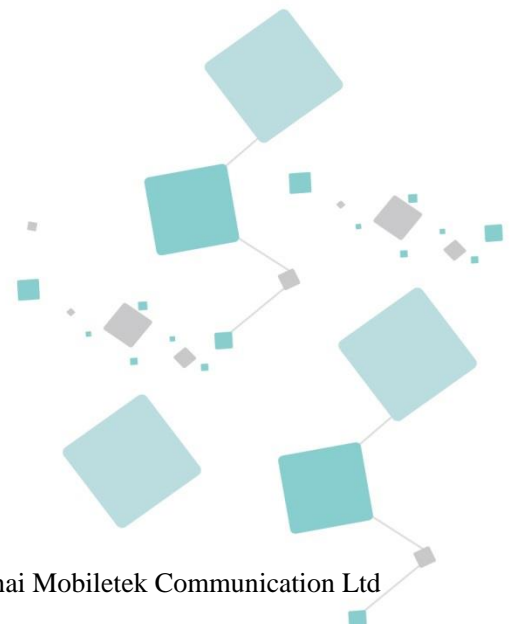


L510-3 Hardware Design

IoT Module Series

Version: V1.0

Date: 2022-03-15



Notice

Some features of this product and its accessories depend on installed software, local network capabilities and settings, and some features may not be activated or restricted due to local network operators or network service providers. As a result, the description in this article may not be an exact match to the product you purchased or its accessories. The company shall not be responsible for the loss of property or personal injury caused by the user's improper operation. The company reserves the right to modify or change the contents of this manual in accordance with the requirements of technological development.

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Version History

Date	Version	Description of change	Author
2022-03-15	V1.0	Initial	hb.fang

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1. About this document

1.1 Applicable scope

This document describes the L510-3 LCC Module (here in after referred to as L510-3), the basic specifications, product electrical characteristics, design guidance and hardware interface development guidance. Users need to follow this documentation requirements and guidance for design.

This document applies only to L510-3 products in the application development.

1.2 Writing purpose

This document provides the design and development basis for the product users. By reading this document, users can have a whole understanding of the product, the technical parameters of the product have a clear understanding, and can be used in this document to complete the development of wireless Internet access functions.

This hardware development document not only provides the product functional features and technical parameters, but also provides product reliability testing and related testing standards, business functions to achieve process, RF performance indicators and user circuit design guidance.

1.3 Support and reference documents list

In addition to the hardware development documentation, we also provide a guide to the development board based on this product manual and software development instruction manual, 1-1 is supported as a list.

Table 1-1 support document list

No.	Documents
1	《L510-3 AT Command User Guide》
2	《L510-3_SPEC.docx》
3	《L510-3 EVB User Manual》
4	《L510-3 EVB User Manual》
5	《L510-3 Schematic checklist》
6	《L510-3 Layout checklist》
7	《L510-3_Reference Design_V1.pdf》
8	《L510-3_V1_DECAL.sch》
9	《L510-3_V1_DECAL.PCB》

1.4 Terms and Abbreviations

Table 1-2 is the Document relative Terms and Abbreviations.

Table 1-2 Terms and Abbreviations

Abbreviation	Descriptions
ESD	Electro-Static discharge
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver Transmitter
SDCC	Secure Digital Card Controller
USIM	Universal Subscriber Identification Module
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit
PCM	Pulse-coded Modulation

I/O	Input/output
LED	Light Emitting Diode
GPIO	General-purpose Input/Output
GSM	Global Standard for Mobile Communications
GPRS	General Packet Radio Service
WCDMA	Wideband Code Division Multi Access
UMTS	Universal Mobile Telecommunication System
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
AGPS	Assisted Global Positioning System
BER	Bit Error Rate
DL	Downlink
COEX	WLAM/LTE-ISM coexistence
SMPS	Switched-mode power supplies
LTE	Long Term Evolution
FDD	Frequency Division Duplexing
TDD	Time Division Duplexing
DPCH	Dedicated Physical Channel
DPCH_Ec	Average energy per PN chip for DPCH. DPCH
PSM	Power Saving Mode

2. Product Overview

L510-3 is a series of LTE CAT1 module and special design for global IOT market, and it's have integrated rich peripheral interface. User can choose the module based on the wireless network configuration. In this document, the supported radio band is described in the following items. This product is a LCC interface of IoT wireless internet module, with the high speed, small size, light weight, high reliability can be widely used in various products and devices with wireless internet access. Please refer to the table below for a detailed description of frequency bands

Table 2-1 L510-3 series models

Band		L510E-3(E/S)	L510EN-3(E/S)
GSM/GPRS	850MHZ	●	●
	900MHZ	●	●
	1800MHZ	●	●
FDD LTE	B1	●	●
	B3	●	●
	B7	●	●
	B8	●	●
	B20	●	●
	B28	●	●
GNSS	GPS		●
	GLONASS		●

RF Parameter

- FDD LTE: B1/B3/B7/B8/B20/B28
- GSM: B3/B8
- GNSS: GPS/GLONASS

Interface

- USB2.0
- UART
- USIM (1.8V)
- GPIO
- ADC
- PCM
- SPI
- I2C
- MIPI_RFFE
- NETLIGHT
- POWER KEY
- WAKEUP_OUT/WAKEUP_IN
- MODULE STATUS

Dimensions (LxWxH) :25mmx21.5mmx2.4mm

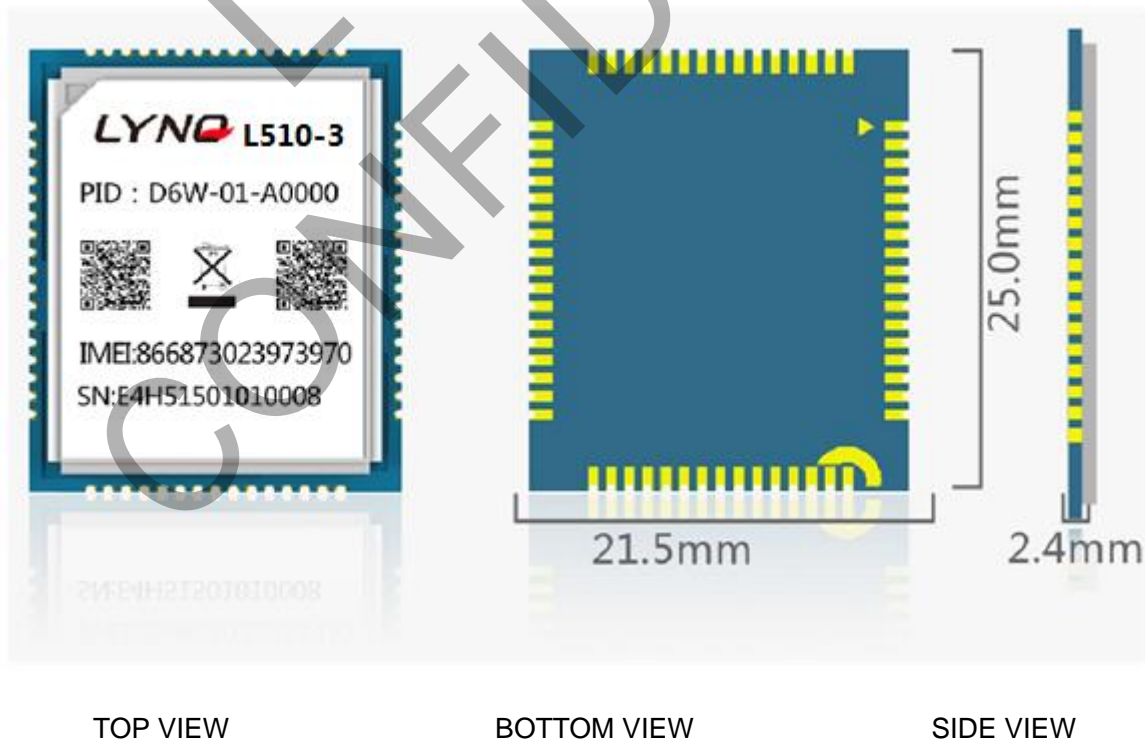
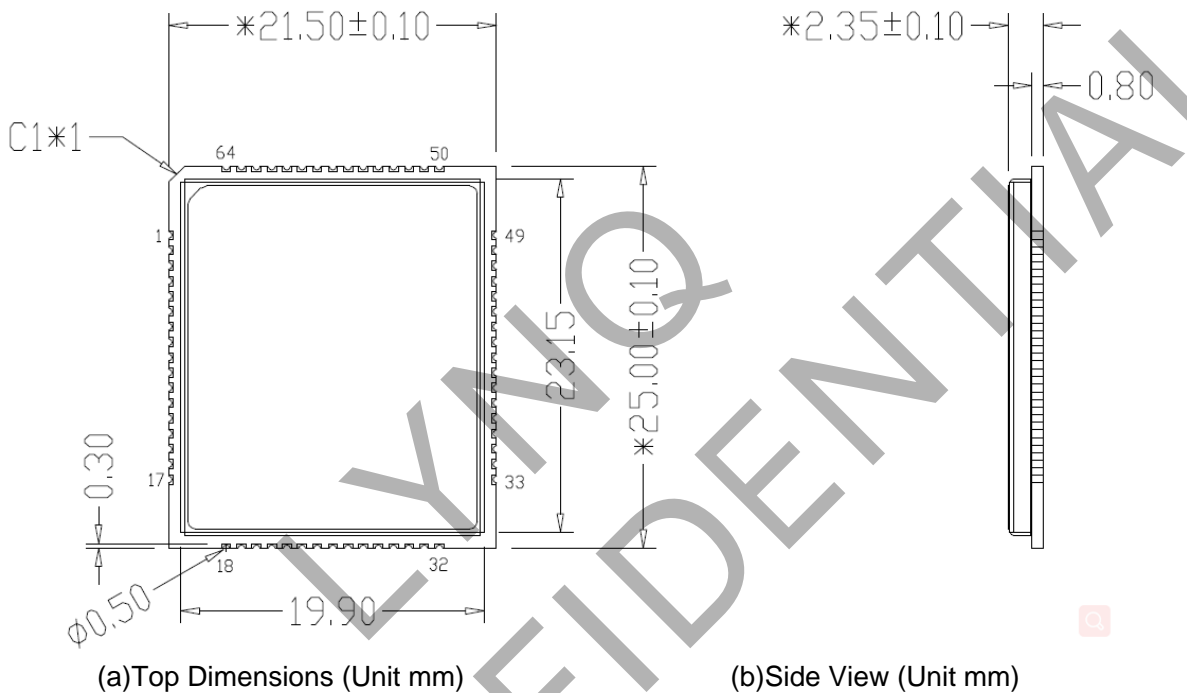
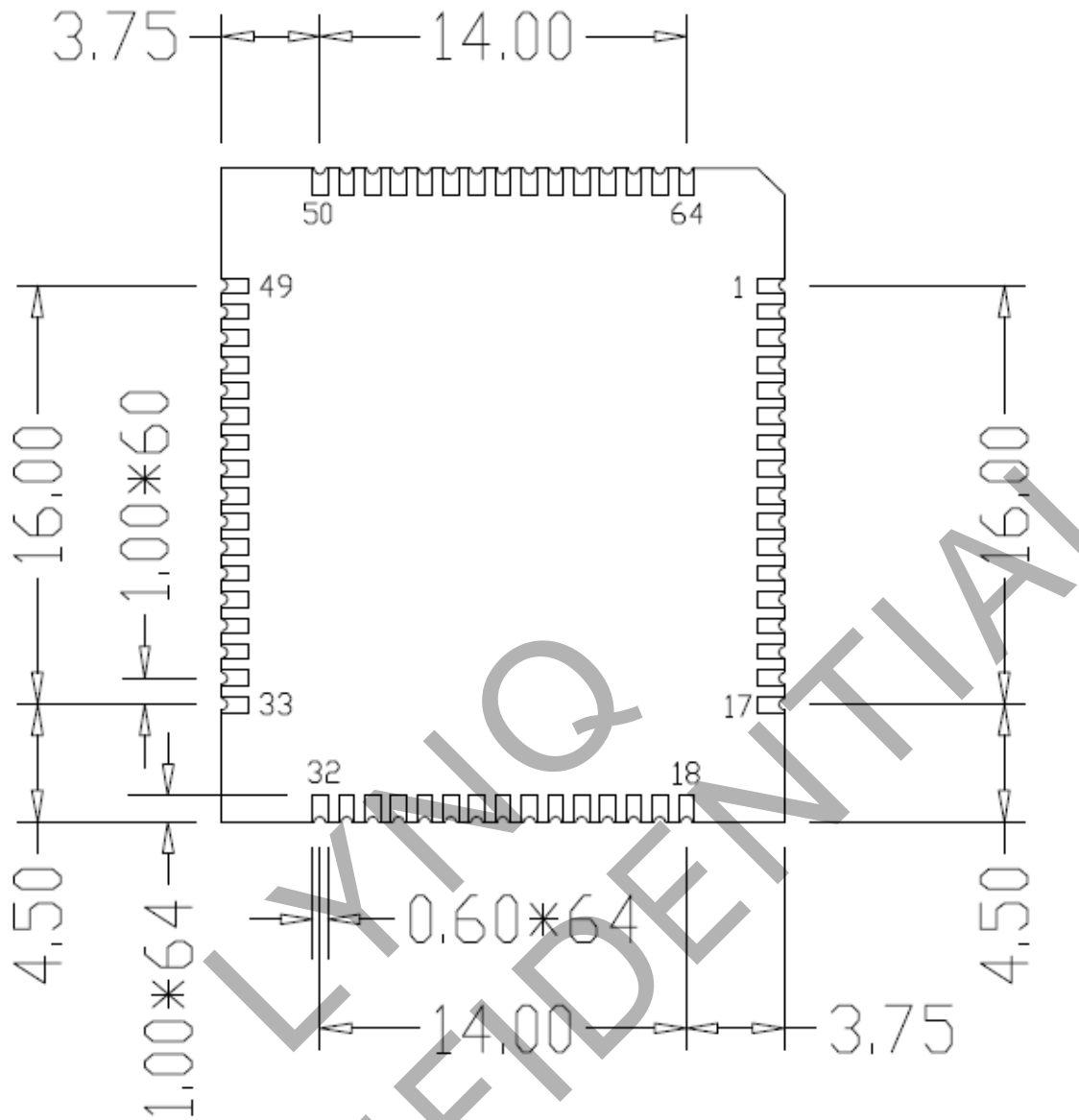


Figure 2-1 Product Physical Map

2.1 Package Dimensions

The product module is 64-PIN LCC package module. The size of L510-3 is extremely small, it is only 21.5.0 x 25.0 x 2.4 mm with LCC package, It is cost competitive and high integrated which make it convenient for customer to design their own application products. Pin 1 position from the bottom of the belt angle welding plate to identify, the missing corner where the direction of the corresponding module angle pad, figure 2-2 is the product dimension type map:





(c)Bottom Dimensions (Unit mm)

Note: For information regarding Footprint and Paste Mask recommended for the application of L510-3

Figure 2-2 Module Dimensions

2.2 Product Function Outline

2.2.1 Hardware Diagram

This product mainly includes the following signal group: USB Interface signal、USIM card Interface signal、I2C Interface signal、UART Interface signal、PCM Interface signal、SPI interface、Module startup、Module control signal、Power supply and ground. The global architecture of the L510-3

module is described in the figure below.

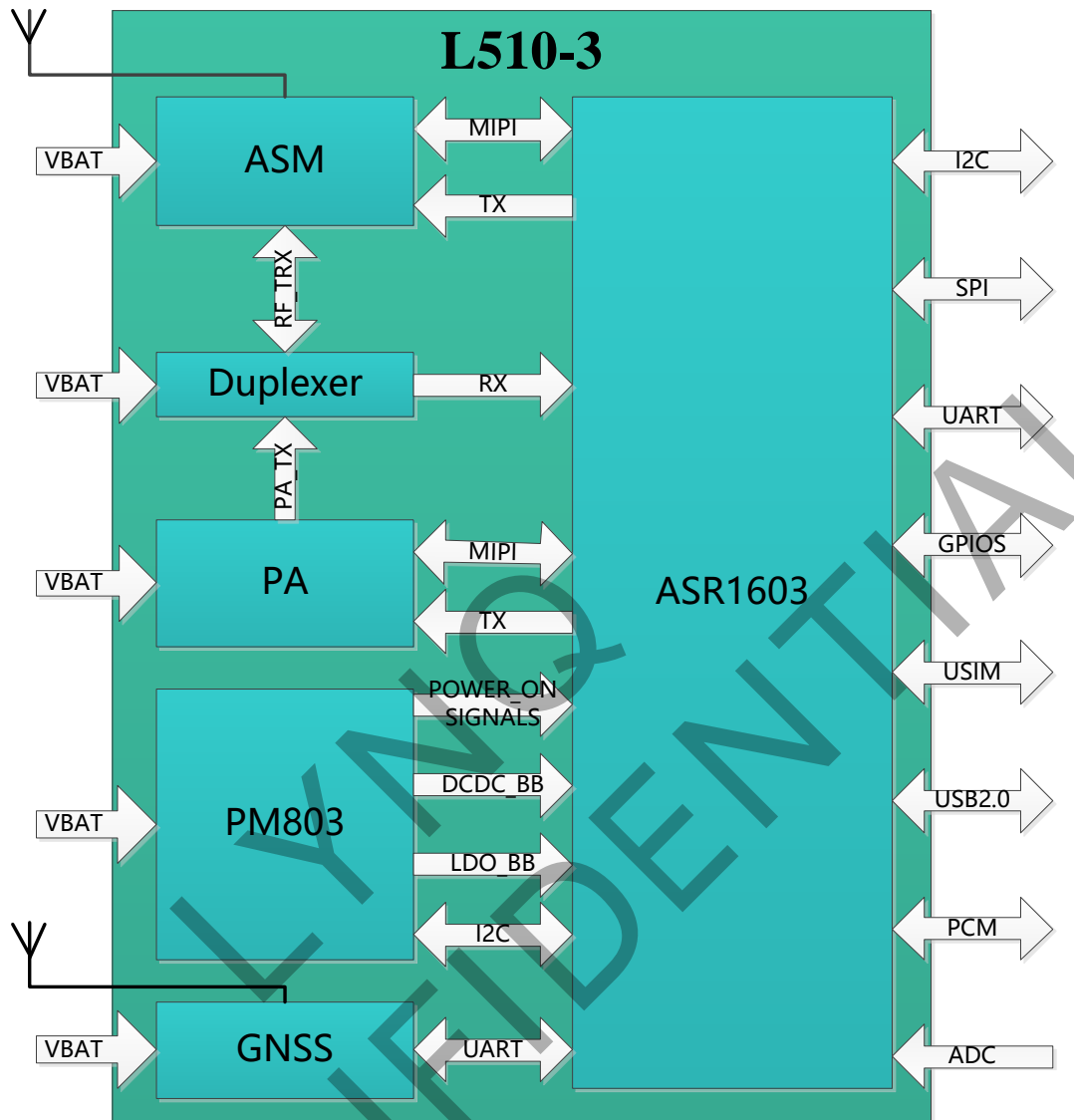


Figure 2-3 L510-3 System Functional Architecture

2.2.2 Radio frequency function

RF Function Overview:

- Multi -Band Half Duplex FDD-LTE Cat1 GNSS
- GSM Band: GSM900 DCS1800

The operating frequency range of the transmitter is shown in table 2-1.

Table 2-2 RF frequency band

Working band	Upstream band (Uplink)	Downlink frequency (Downlink)
FDD_LTE B1	1920 MHz~1980 MHz	2110 MHz~2170 MHz
FDD_LTE B3	1710 MHz~1785 MHz	1805 MHz~1880 MHz
FDD_LTE B7	2500 MHz~2570 MHz	2620 MHz~2690 MHz
FDD_LTE B8	880 MHz~915 MHz	925 MHz~960 MHz
FDD_LTE B20	832 MHz~862 MHz	791 MHz~821 MHz
FDD_LTE B28	703 MHz~748 MHz	758 MHz~803 MHz
GSM900	890 MHz — 915MHz	925 MHz — 960MHz
DCS1800	1710 MHz — 1785MHz	1805 MHz — 1880MHz
GPS L1 BAND		1574.4 ~ 1576.44 MHz
GLONASS		1598 ~ 1606 MHz

Table 2-3 L510-3 Conducted transmission power

Working Band	Max Power	Min Power
FDD_LTE B1	20dBm +/-2.7dB	<-40dBm
FDD_LTE B3	20dBm +/-2.7dB	<-40dBm
FDD_LTE B7	20dBm +/-2.7dB	<-40dBm
FDD_LTE B8	20dBm +/-2.7dB	<-40dBm
FDD_LTE B20	20dBm +/-2.7dB	<-40dBm
FDD_LTE B28	20dBm +/-2.7dB	<-40dBm
GSM900	33dBm ±2dB	5dBm ± 5dB
DCS1800	30dBm ±2dB	0dBm ± 5dB
GSM900(8-PSK)	27dBm ±3dB	5dBm ± 5dB
DCS1800(8-PSK)	26dBm +3/-4dB	0dBm ± 5dB

Table 2-6 L510-3 Reference sensitivity (QPSK)

Channel bandwidth					
E-UTRA Band	200 KHz (CAT NB1) REF SENS (Total)	200 KHz (CAT NB1) REF SENS (EPRE @15KHz)	200 KHz (CAT NB1) NB-PDSCH repetitions (Total)	200 KHz (CAT NB1) NB-PDSCH repetitions (EPRE @15KHz)	Duplex Mode
1	-113	-123.8	TBD	= Total – 10.8dBm	HD-FDD
3	-113	-123.8	TBD	= Total – 10.8dBm	HD-FDD
7	-114	-124.8	TBD	= Total – 10.8dBm	HD-FDD
8	-114	-124.8	TBD	= Total – 10.8dBm	HD-FDD
20	-114	-124.8	TBD	= Total – 10.8dBm	HD-FDD
28	-114	-124.8	TBD	= Total – 10.8dBm	HD-FDD

3. Interface Description

3.1 PIN Definition

3.1.1 Pin I/O parameter definition

The I/O parameter definition of the product is shown in table 3-1.

Table 3-1 I/O parameter definitions

Pin attribute symbol	Description
PI	Power input PIN
PO	Power output PIN
AI	Analog input
AIO	Analog signal input/output PIN
I/O	Digital signal input/output PIN
DI	Digital signal input
DO	Digital signal output
DOH	Digital output with high level
DOL	Digital output with low level
PD	Pull down
PU	Pull up
AO	Analog output

3.1.2 Pin Map

L510-3 is an extremely small LCC package module and special designed for the IOT marketing, and it have integrated rich peripheral interface. Such as SIM, USB , PCM ,UART and interactive interface,

detail description show as below chart. All hardware interfaces which connect L510-3 to customers' application platform are through 64 pins pads (Metal half hole). Figure 3-1 is L510-3 PIN outline diagram.

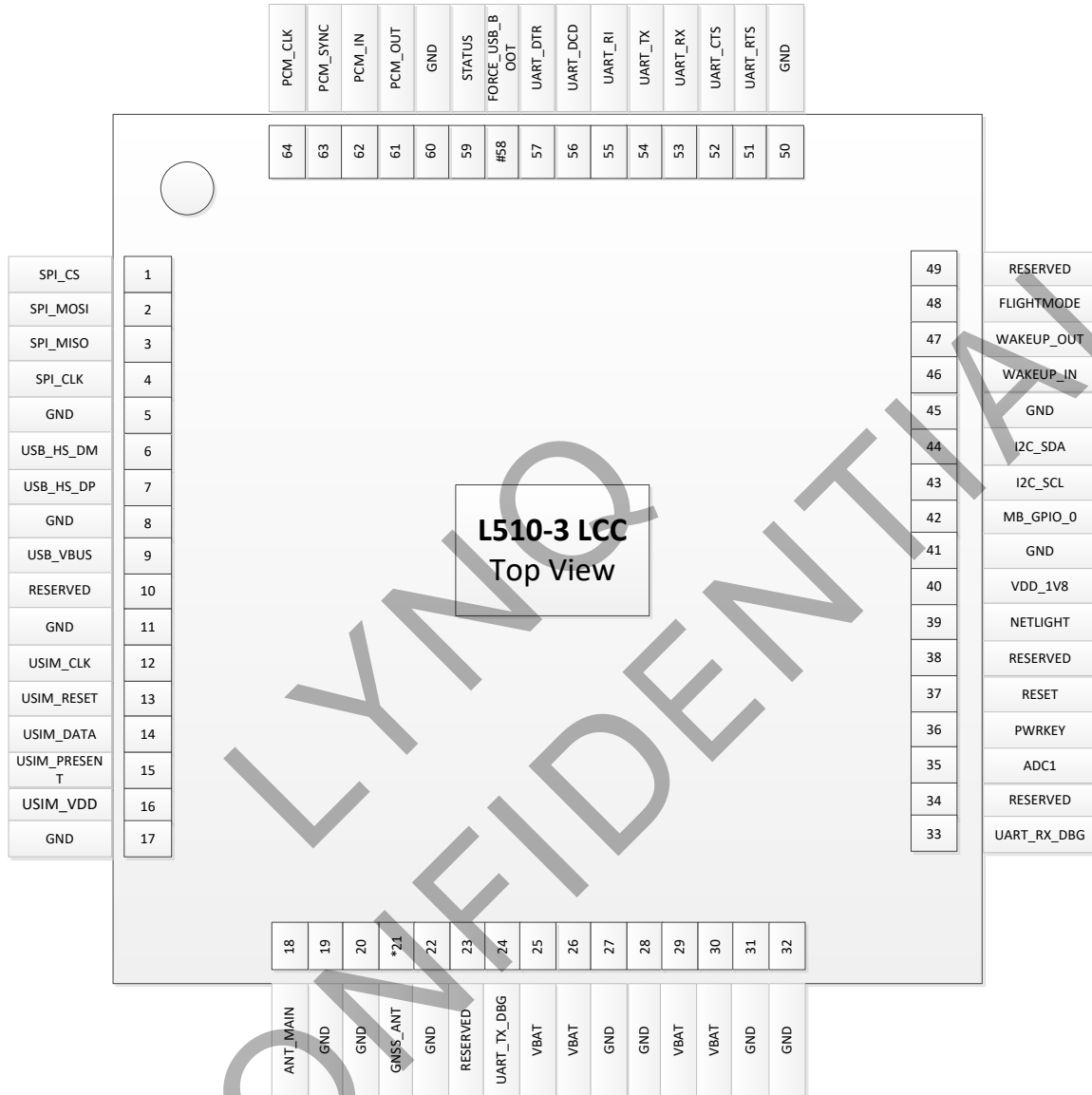


Figure 3-1 Pin Map View (Top View)

Note:1. # flag Pin standard this pin is a Multi-function pin and it's integrated different function in different system status, and the detail function please refer to the correspond chapter.

2. The * mark pin, different version function definition is different, do not use to no connection, and the detail function please refer to the correspond chapter.

3.1.3 PIN Definition and function description

Table 3-2 Pin definition

Pin No.	Pin description	Pin No.	Pin description
1	SPI_CS	2	SPI_MOSI
3	SPI_MISO	4	SPI_CLK
5	GND	6	USB_HS_DM
7	USB_HS_DP	8	GND
9	USB_VBUS	10	RESERVED
11	GND	12	USIM_CLK
13	USIM_RESET	14	USIM_DATA
15	USIM_PRESENT	16	USIM_VDD
17	GND	18	ANT_MAIN
19	GND	20	GND
*21	GNSS_ANT	22	GND
23	RESERVED	24	UART_TX_DBG
25	VBAT	26	VBAT
27	GND	28	GND
29	VBAT	30	VBAT
31	GND	32	GND
33	UART_RX_DBG	34	RESERVED
35	ADC1	36	PWRKEY
37	RESET	38	RESERVED
39	NETLIGHT	40	VDD_1V8
41	GND	42	MB_GPIO_0
43	I2C_SCL	44	I2C_SDA

45	GND	46	WAKEUP_IN
47	WAKEUP_OUT	48	FLIGHTMODE
49	RESERVED	50	GND
51	UART_RTS_N	52	UART_CTS_N
53	UART_RX	54	UART_TX
55	UART_RI	56	UART_DCD
57	UART_DTR	#58	FORCE_USB_BOOT
59	STATUS	60	GND
#61	PCM_OUT	#62	PCM_IN
#63	PCM_SYNC	#64	PCM_CLK

Note: The # marker pin is a reuse function pin, that is, the pin is a multi-purpose function pin and has some special purposes in addition to the marked functions, as detailed in the interface description.

*Note: the * mark pin, different version function definition is different, do not use to no connection, and the detail function please refer to the correspond chapter.*

Table 3-3 Pin Function Description

Power interface				
Pin Name	Pin No.	I/O	Description	Content
VBAT	25,26,29,30	PI	Power supply voltage, VBAT=3.4V~4.2V.	The power supply for system Maximum load current must above 2A. Keep de-cap capacitor close to the this Net.
USIM_VDD	16	PO	Module LDO output power, single-voltage 1.8V output, Max current 50mA.	Only use for external SIM Card VDD.
VDD_1V8	40	PO	Module LDO output power for MCP and accessories	If not use please let it open or add a 10 UF de-cap capacitor to

				ground.
GND	5,8,11,17,1 9,20,22,27, 28,31,32,4 1,45,50,60	--	Ground.	
System control interface				
Pin Name	Pin No.	I/O	Description	Content
PWRKEY	36	DI	System power on/off input, active low. Long Key to achieve reset function.	
FLIGHTMODE	48	DI	The input signal, used to control the system into flight mode, L: flight mode; H: normal mode	
RESET	37	DI	Lower the module for 1S and release, the module hardware reset	
Interactive interface				
Pin Name	Pin No.	I/O	Description	Content
NETLIGHT	39	DO	Identify the system network status.	If not use keep it open.
STATUS	59	DO	Module status identify: High level power on, low level power off.	If not use keep it open.
WAKEUP_IN	46	DI	AP weak up module	
WAKEUP_OUT	47	DO	Module wake up AP	
SIM interface				
Pin Name	Pin No.	I/O	Description	Content
UIM_DATA	14	I/O	USIM Card data I/O, which has been pulled up with a 10KR resistor to USIM_VDD in module. Do not pull up or pull down in users' application circuit.	All signals of USIM interface should be protected with ESD/EMC.
UIM_RESET	13	DO	UIM Reset	

UIM_CLK	12	DO	UIM Clock	
USIM_VDD	16	PO	UIM Card Power output, output, only support 1.8V SIM Current is less than 50mA.	
USIM_PRESEN T	15	DI	USIM hot-plug detection (default low level valid)	
SPI interface				
Pin Name	Pin No.	I/O	Description	Content
SPI_CS	1	DO	SPI_CS ,SPI chip select	If not use keep it open.
SPI_MOSI	2	DO	SPI master-out slave-in	
SPI_MISO	3	DI	SPI master-in slave-out	
SPI_CLK	4	DO	SPI CLOCK	
PCM interface				
Pin Name	Pin No.	I/O	Description	Content
PCM_OUT	61	DO	PCM_OUT, PCM data output	PCM signals can be reused as I2S signals
PCM_IN	62	DI	PCM_IN, PCM data input	
PCM_SYNC	63	DO	PCM_SYNC, PCM data frame sync signal	
PCM_CLK	64	DO	PCM_CLK, PCM data bit clock	
FULL UART				
Pin Name	Pin No.	I/O	Description	Content
RTS	51	DI	DET Request to send.	If not use keep it open.
CTS	52	DO	Clear to Send.	If not use keep it open.
RX	53	DI	Receive Data.	If not use keep it open.
TX	54	DO	Transmit Data.	If not use keep it open.
RI	55	DO	Ring Indicator.	If not use keep it open.
DCD	56	DO	Carrier detects.	If not use keep it open

DTR	57	DI	DTE get ready.	If not use keep it open.
DEBUG PORT				
Pin Name	Pin No.	I/O	Description	Content
UART_TX_DBG	24	DO	LOG for DEBUG	If not use, it is recommended to reserve test points
UART_RX_DBG	33	DI	LOG for DEBUG	
I2C interface				
Pin Name	Pin No.	I/O	Description	Content
I2C_SCL	43	DO	I2C clock output.	If not use keep it open.
I2C_SDA	44	I/O	I2C data input/output.	
RF port				
Pin Name	Pin No.	I/O	Description	Content
MAIN_ANT	18	AIO	Main Antenna	
GNSS_ANT	*21	AI	GNSS Antenna	
Others				
Pin Name	Pin No.	I/O	Description	Content
ADC1	35	AI	Analog conversion digital input interface1	If not use keep it open.
FORCE_USB_BOOT	58	DI,PD; I/O	Pull up to 1.8V (L510-3 VDD_1V8) with 10K resistor force module in USB download mode	Recommend placing test points for debug.
RESERVED	10,23,34,38,49		Reserved for other purposes	Keep them open

3.2 Operating condition

Table 3-4 module recommended operating condition

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Main power supply for	3.3	3.8	4.5	V

	the module				
--	------------	--	--	--	--

3.3 Digital I/O characteristics

Table 3-5 1.8V Digital I/O characteristics

Parameter	Description	Min.	Max.	Unit
V _{IH}	High level input voltage	0.7*VDD_PX	VDD_PX+0.2	V
V _{IL}	Low level input voltage	-0.3	0.3* VDD_PX	V
V _{OH}	High level output voltage	VDD_PX-0.2	-	V
V _{OL}	Low level output voltage	-	0.2	V
I _{OH}	High-level output current (no pull down resistor)	-	-	mA
I _{OL}	Low-level output current (no pull up resistor)	-	-	mA
I _{IH}	Input high leakage current (no pull down resistor)	-	1	uA
I _{IL}	Input low leakage current (no pull up resistor)	-1	-	uA

*Note: 1. These parameters are for digital interface pins, such as SPI, I2C, GPIOs, UART, PCM, SIM.

2. VDD_PX=VDD_1V8, unless otherwise noted

3.4 Power Interface

3.4.1 Power supply pin description

Table 3-6 DC Power Characteristics

Pin No.	Net Name	Description	DC Characteristic (V)
---------	----------	-------------	-----------------------

			Min.	Typ.	Max.
25,26,29,30	VBAT	Power supply for the module RF	3.3	3.8	4.5
5,8,11,17,19,20,22,27,28,31,32,41,45,50,60	GND	GND	-	-	-

3.4.2 Power supply requirements

There are four VBAT PIN power for the module, VBAT directly power supply for the module baseband and PA, and operating rating is 3.3V~4.5V; In the weak network environment, the antenna will be maximum power emission. Voltage must be stable, because during operation the current drawn from VCC may vary significantly.

Table 3-7 VBAT power supply interface characteristics

Symbol	Description	Min	Typ	Max	Unit
VBAT	Power supply voltage	3.3	3.8	4.5	V
IVBAT(peak)	Power supply p current	-	-	2000	mA
IVBAT(average, Power Saving Mode disabled, Module registered with network)	Power supply average current	-	14	-	mA
IVBAT(power-off)	Power supply current in power off mode	-	17	-	uA
IVBAT(power-save mode)	Power supply current in power save mode(Deep sleep mode)	-	7	-	uA

3.4.3 Power Supply Design Guide

Make sure that the input voltage at the VBAT pin will never drop below 3.3V even during a transmit burst when the current consumption rises up to more than 2 A. If the power voltage drops below 3.3V, the RF performance of module may be affected. Using large tantalum capacitors (above 300uF) will be the best way to reduce the voltage drops. If the power current cannot support up to 2 A, users must introduce larger capacitor (typical 1000uF) to storage electric power. For the consideration of

RF performance and system stability, some multi-layer ceramic chip (MLCC) capacitors (0.1/1uF) need to be used for EMC because of their low ESR in high frequencies. Note that capacitors should be put beside VBAT pins as close as possible. Also User should keep VBAT net wider than 2 mm to minimize PCB trace impedance on circuit board. The following figure is the recommended circuit.

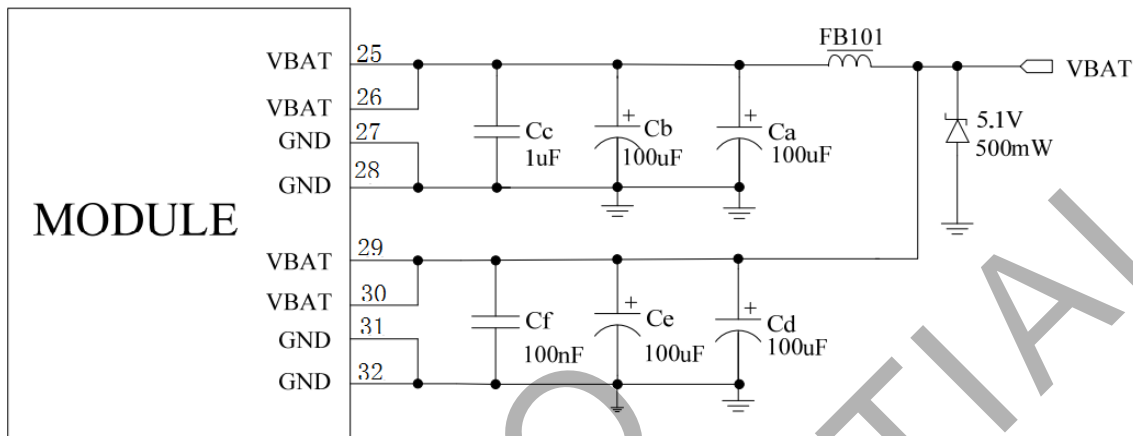


Figure 3-2 VBAT input application circuit

Note: The Cd, Ce, Cb, Cc and Cf are recommended being mounted for L510-3, but the Ca, Cb, Ce, Cc and Cf for tune.

In addition, in order to get a stable power source, it is suggested to use a Zener diode of which reverse Zener voltage is 5.1V and dissipation power is more than 500mW. Some zener diodes will have leakage of 1uA, which will increase the power consumption in PSM mode.

Table 3-8: Recommended Zener diode models

NO.	Manufacturer	Part Number	Power	Package
1	On semi	MMSZ5231BT1G	500mW	SOD123
2	Prisemi	PZ3D4V2H	500mW	SOD123
3	Vishay	MMSZ4689-V	500mW	SOD123

3.4.4 Recommended Power supply circuit

If the voltage difference is not big, we recommend DCDC or LDO is used for the power supply of the module, make sure that the peak current of power components can rise up to more than 2 A. The following figure is the reference design of +5V input linear regulator power supply. The designed output for the power supply is 3.8V.

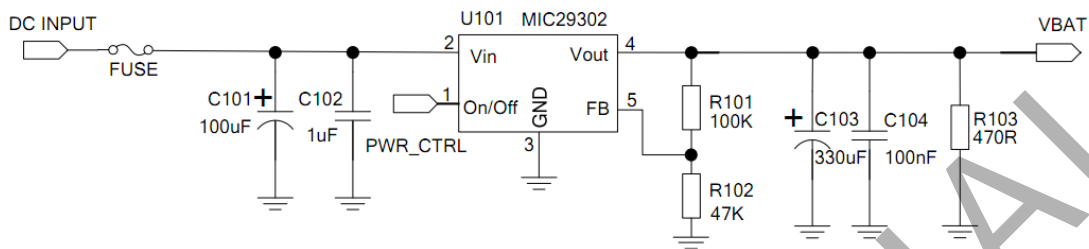


Figure 3-3 Reference circuit of the LDO power supply

If there is a big difference between the input voltage and the desired output (VBAT) or better efficiency is more important, a switching converter power supply will be preferable. The following figure is the reference circuit.

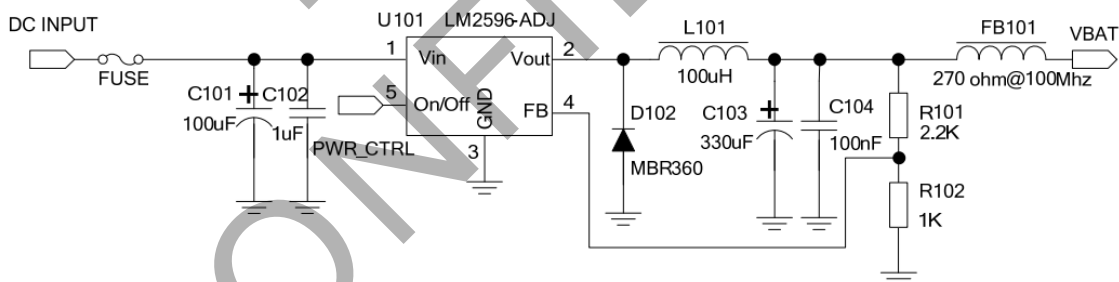


Figure 3-4 Reference circuit of the DCDC power supply

Note: DCDC may deprave RF performance because of ripple current intrinsically.

3.4.5 Power Supply Layout guide

The layout of the power supply section and the related components is of vital importance in the power

module design. If processes this part layout is not good, will lead to various effects, such as bad EMC, effective the emission spectrum and receiving sensitivity, etc. So the power supply part design is very important, when you design this part you should notes below contents: 1. DC DC switch power should place away from the antenna and other sensitivity circuit; 2. Consider the voltage drop and the module current requirement, the layout line should better above 100mil. If conditions allow should add a power shape plane.

3.5 UIM interface

3.5.1 Pin definition

The L510-3 integrated a ISO 7816-2 standard USIM port, and only 1.8V SIM Cards are supported.

Table 3-9(a) (U)SIM card signal group definition and description

Pin No.	Signal name	I/O Type	Descriptions
16	USIM_VDD	UIM Card Power output	
14	USIM_DATA	USIM Card data I/O, which has been pulled up with a 10KR resistor to USIM_VDD in module. Do not pull up or pull down in users' application circuit.	
12	USIM_CLK	SIM clock signal	
13	USIM_RST	SIM reset signal	

Table 3-9 (b) UIM Electronic characteristic (USIM_VDD =1.8V)

Symbol	Parameter	Min.	Ty p.	Max.	Unit
USIM_VDD	LDO power output	1.75	1.8	1.85	V
VIH	High-level input voltage	0.65·USIM_VDD	-	USIM_VDD +0.3	V
VIL	Low-level input voltage	-0.3	0	0.35·USIM_VDD	V

VOH	High-level output voltage	USIM_VDD -0.45	--	USIM_VDD	V
VOL	Low-level output voltage	0	0	0.45	V

3.5.2 Design Guide

In order to meet the 3 GPP TS 51.010 1 protocol and EMC certification requirements. Suggest UIM slot near the location of the module USIM card interface, to avoid running for too long, lead to serious deformation of waveform and effect signal integrity, UIM_CLK and UIM_DATA signal lines suggest ground protect. Between the UIM VCC & GND add a 1uF and a 33 pF capacitor in parallel, Between the SIM_CLK& GND, UIM_RST& GND, UIM DATA& GND add a 33 pF capacitor in parallel, for filter the RF signal interference.

3.5.3 UIM interface reference circuit

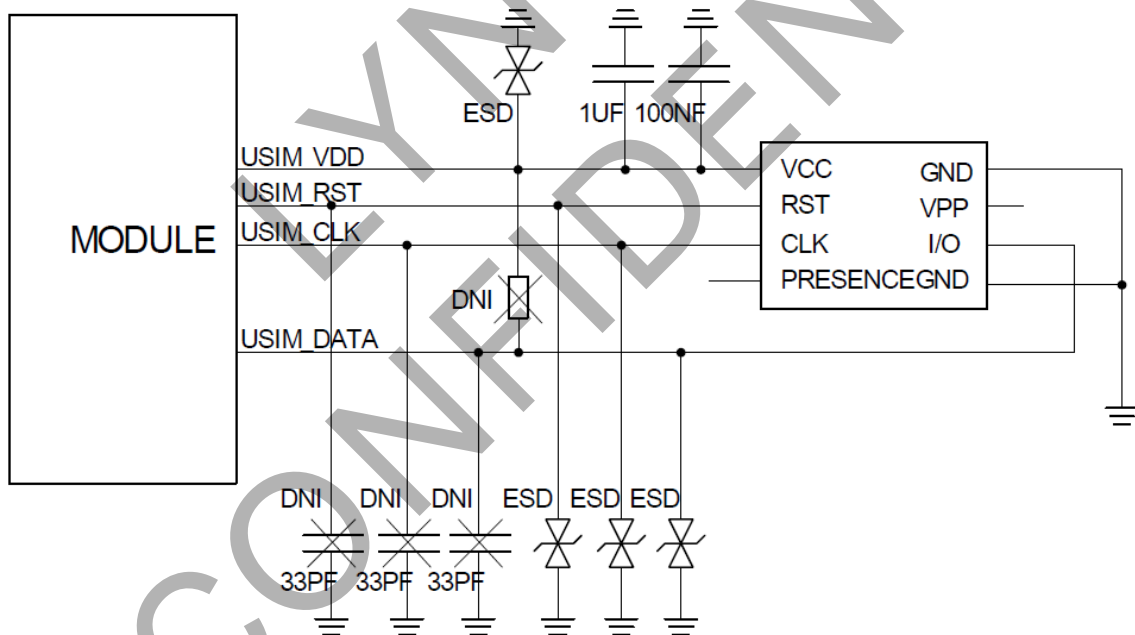


Figure 3-6 UIM Reference circuit

Note: UIM_DATA have added the pull-up resistance in the module design.

3.6 PCM interface(TBD)

3.6.1 PCM interface definition

L510-3 provides hardware PCM interface for external codec. L510-3 PCM interface can be used in short sync master mode only, and only supports 16 bits linear format:

Table 3-10 (a) PCM interface definition

Pin No.	Signal name	I/O Type	DC Characteristics (V)		
			Min.	Typ.	Max.
63	PCM_SYNC	PCM synchronizing signal	-0.3	1.8	1.9
62	PCM_DIN	PCM data input	-0.3	1.8	1.9
61	PCM_DOUT	PCM Data output	-0.3	1.8	1.9
64	PCM_CLK	PCM Data clock	-0.3	1.8	1.9

Note: PCM can be used for I2S and TDM

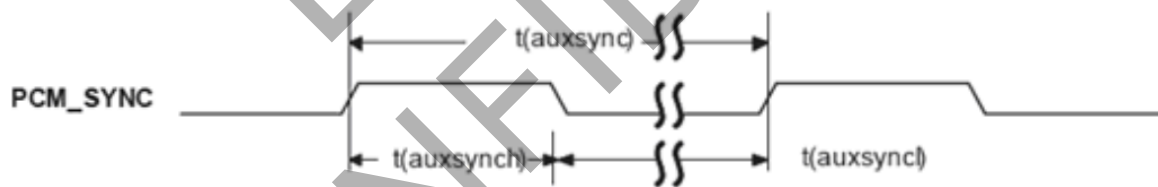


Figure 3-6 PCM_SYNC timing

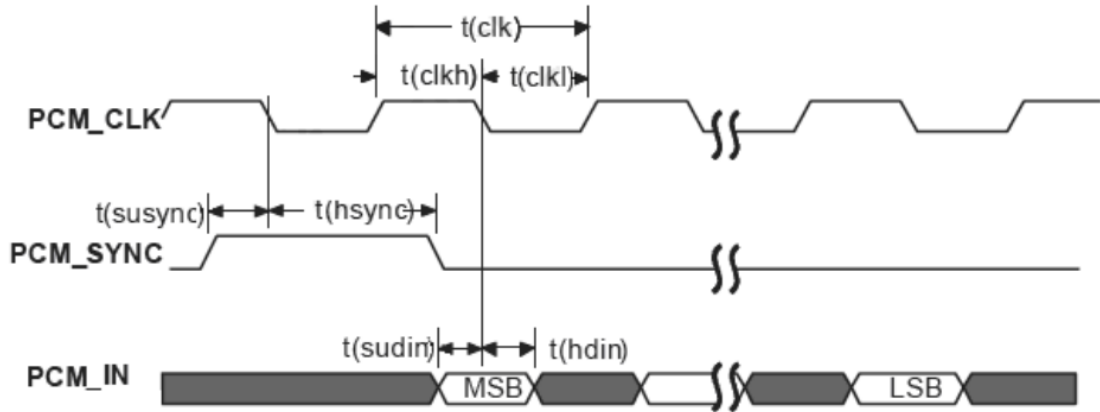


Figure 3-7 Codec to L510-3 module timing

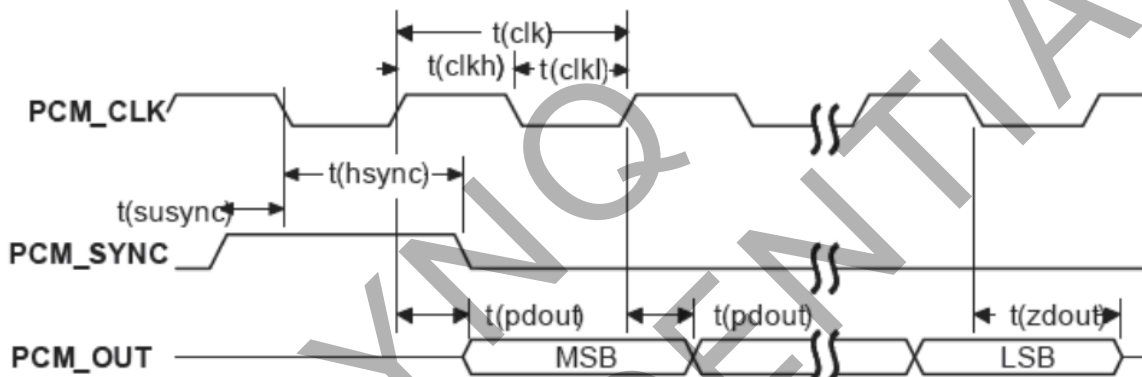


Figure 3-8 L510-3 to codec module timing

Table 3-10 (b) PCM interface Timing

Parameter	Descriptions	DC characters			
		Min.	Typ.	Max.	Unit
T(sync)	PCM_SYNC cycle	-	125	-	us
T(sync _h)	PCM_SYNC high level hold time	-	488	-	ns
T(sync _l)	PCM_SYNC low level hold time	-	124.5	-	us
T(clk)	PCM_CLK cycle	-	488	-	ns
T(clk _h)	PCM_CLK high level hold time	-	244	-	ns
T(clk _l)	PCM_CLK low level hold time	-	244	-	ns

T(susync)	PCM_SYNC establish time	-	122	-	ns
T(hsync)	PCM_SYNC hold time	-	366	-	ns
T(sudin)	PCM_IN establish time	60	-	-	ns
T(hdin)	PCM_IN hold time	60	-	-	ns
T(pdout)	From PCM_CLK rising edge to PCM_OUT valid time	-	-	60	ns
T(zdout)	From PCM_CLK falling edge to PCM_OUT high impedance delay time	-	-	60	ns

3.6.2 PCM interface application

L510-3 only support the host mode, PCM_SYNC, PCM_CLK is the output pin, PCM_SYNC as the synchronizing output 8kHz sync signal. PCM Data support 8bit or 16bit data.

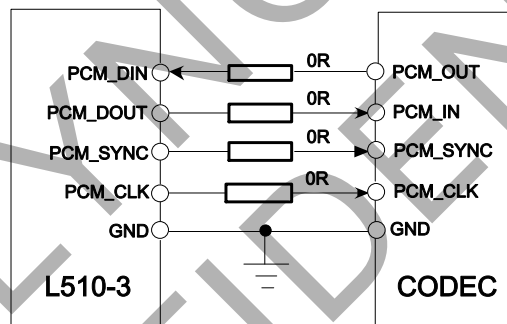


Figure 3-19 PCM application circuit (L510-3 only support in host mode)

Note:1. L510-3 PCM port DC character is base on 1.8 voltage, please pay attention the voltage matching.

2. L510-3 default design base on NAU8814 as the codec chip, the detail design please refer to 《L510-3 reference design》.

3.7 USB2.0 interface

3.7.1 USB interface pin definition

L510-3 module include a high-speed USB 2.0 compliant interface with maximum 480 Mb/s data rate according to USB 2.0 specification, representing the main interface for transferring high speed data with a host application processor. The module itself acts as a USB device and can be connected to any USB host equipped with compatible drivers.

The USB is the most suitable interface for transferring full speed data between module and a host processor, available for AT commands, data communication, FW upgrade, Below table is the module USB pin definition:

Table 3-11 USB interface pin definition

Pin No.	Signal name	I/O type	DC characteristic (V)		
			Min.	Typ.	Max.
6	USB_DM	USB2.0 date D-	-	-	-
7	USB_DP	USB2.0 data D+	-	-	-

3.7.2 USB Interface application

USB bus is mainly used for data transmission, software upgrading, module testing. Work in the full-speed mode of the USB line, if you need ESD design, ESD protection device must meet the junction capacitance value <math>< 5\text{pF}</math>, otherwise the larger junction capacitance will cause waveform distortion, the impact of bus communication. Differential impedance of differential data line in 90ohm + 10%.

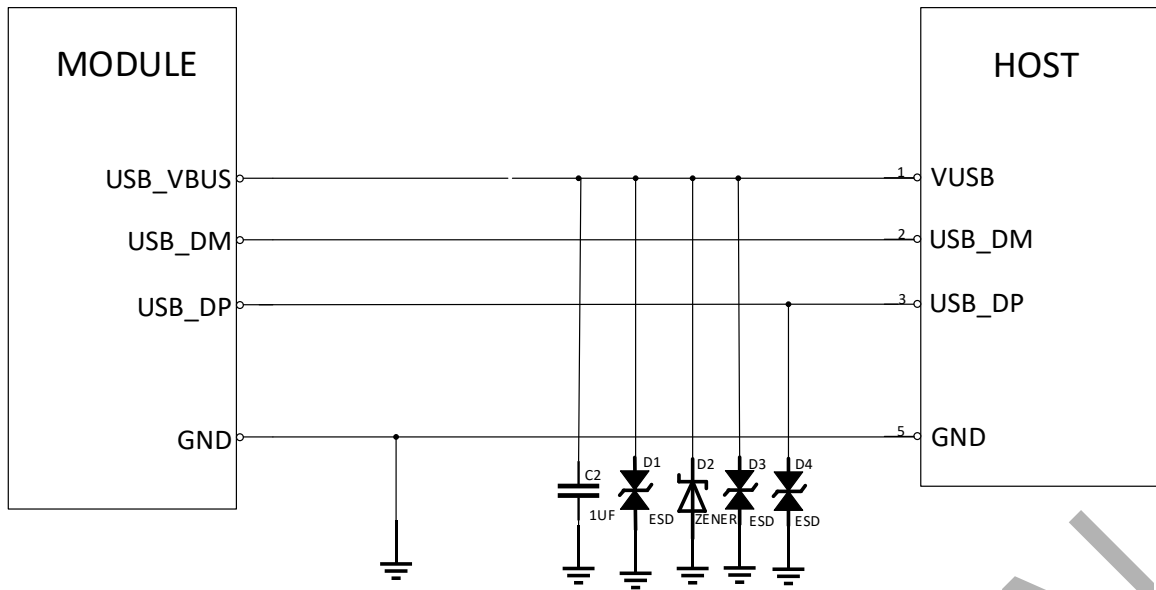


Figure 3-10 USB application

3.8 UART Interface

3.8.1 Pin description

L510-3 module provides a flexible 7-wire UART (universal asynchronous serial transmission) interface. UART as a full asynchronous communication interface, Support the standard modem handshake signal control, Comply with the RS - 232 interface protocols. And also support four wire serial bus interface or the 2-wire serial bus interface mode, and the module can be through the UART interface for serial communication with the outside (DET) and the AT command input, etc. L510-3 module is a DCE (Data Communication Equipment) and client PC is a DTE (Data Terminal Equipment).AT commands are entered and serial communication is performed through UART interface. The pin signal is defined as shown in below table.

Table 3-12 UART pin definition

Pin No.	Pin	I/O type	Descriptions
54	UART_TX	DO	UART data transmission
53	UART_RX	DI	UART data receive

55	UART_RI	DO	Ring Indicator.
51	UART_RTS	DO	UART DET request to send
57	UART_DTR	DI	DTE get ready.
52	UART_CTS	DI	UART Clear to Send.
56	UART_DCD	DO	UART Carrier detects.

3.8.2 UART interface application

L510-3 UART is COMS 1.8V level, Complete serial port with RS-232 functionality conforming to the ITU-T V.24 Recommendation, with CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V for high data bit or OFF state), if the AP voltage level is not the 1.8V should add a voltage transfer module in your application. Below is RS-232 voltage transfer module application diagram.

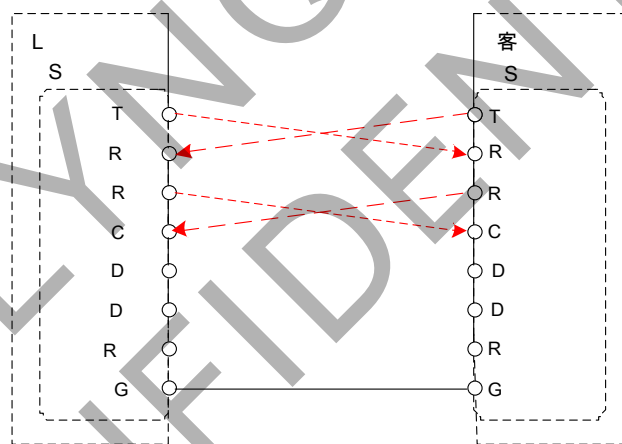


Figure 3-11 UART 4 Line connection mode

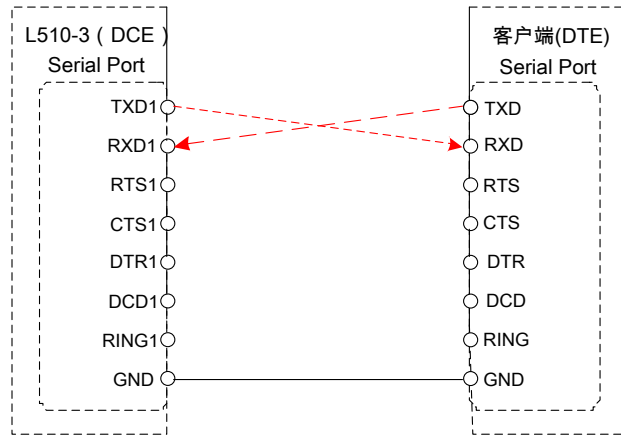


Figure 3-12 UART 2 Line connection mode

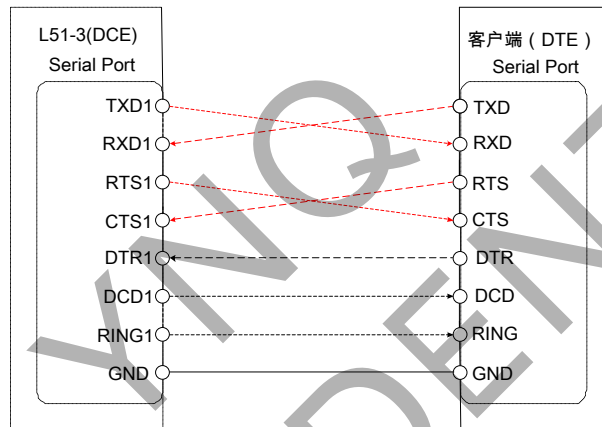
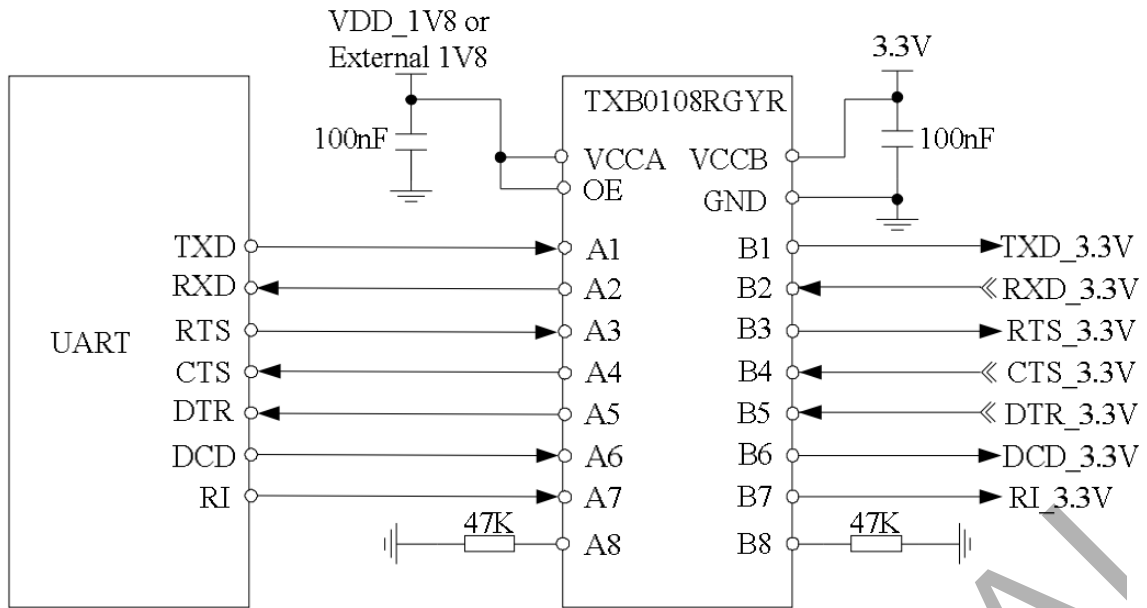


Figure 3-13 UART Full mode

The L510-3 UART is 1.8V interface. A level shifter should be used if user's application is equipped with a 3.3V UART interface. The level shifter TXB0108RGYR provided by Texas Instruments is recommended. The reference design of the TXB0108RGYR is in the following figures. About the application as below:



Figures 3-14 Voltage transfer Reference Circuit

3.9 Power on/off and reset interface

3.9.1 Pin definition

Table 3-13 power on/off and reset key define

Pin No.	Net name	I/O Typ.	descriptions
36	PWRKEY	DI	L510-3 power on/off pin (internal pull-up)
37	RESET	DI	L510-3 reset pin

3.9.2 Power on sequence

Pull down the PWRKEY pin and input a low pulse of about 1s to the boot signal. Then suspend or pull up the pin to start the machine.

POWERKEY grounding, module can realize automatic boot.

3.9.3 Power off sequence

The following methods can be used to power down. These procedures will make module disconnect from the network and allow the software to enter a safe state, and then save data before completely powering the module off.

- Method 1: Power off L510-3 using the PWRKEY pin more than 3 seconds.
- Method 2: Power off L510-3 by AT command “AT+CPOF”

Note: 1. About the AT command “AT+CPOF” detail please refer document [1].

2. Over-voltage or under-voltage may cause automatic power down.

3. Over-temperature or under-temperature may cause automatic power down.

Note: the STATUS pin can be used to identify whether has been power on, when the module has access to electricity and initialization is completed, the STATUS output high level, or has maintained low level.

3.9.4 Force PSM mode Out

When the L510-3 in PSM (Power saving mode) you can force the module to exit PSM mode by pulling down the PWRKEY pin. About how to enter the PSM please refer the L510-3 AT command user manual.

3.9.5 Reset sequence

Pin 37 of the module is the hardware reset pin. When the RESET pin is entered a low level lasting 1 second, the module will restart. There is a pull-up inside the system, with a typical value of 1.8V, without the need for external pull-up.

Note: it is recommended that only in an emergency, such as module without response, use the RESET function.

3.9.6 Power on/off interface application

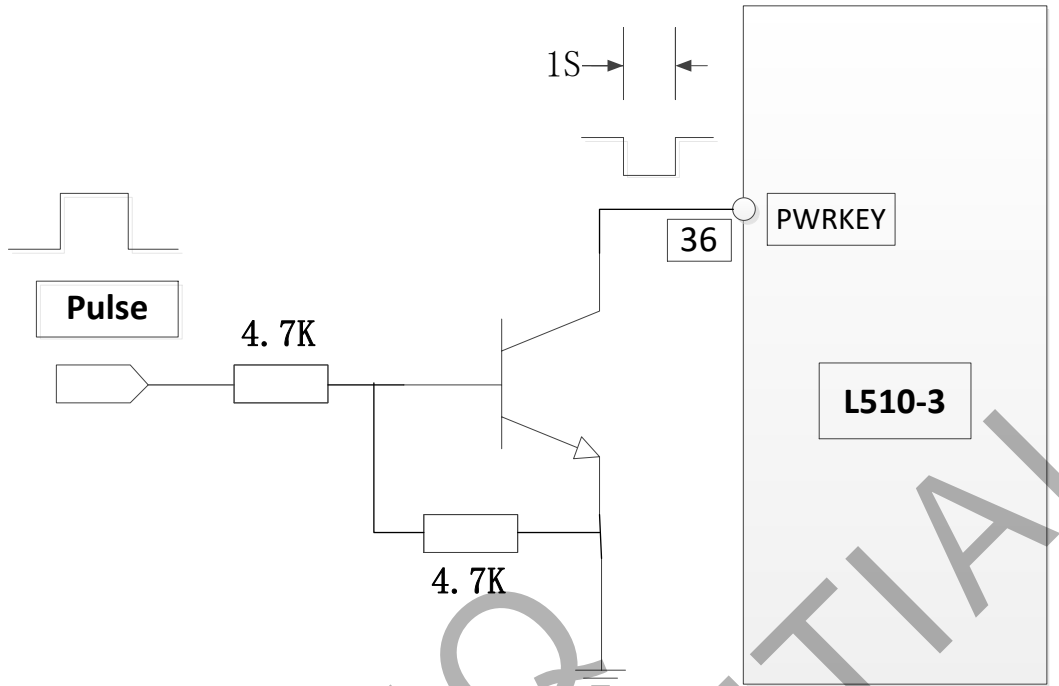


Figure 3-17: Reference power on/off circuit

Another way to control the PWRKEY pin is directly using a push button switch. Need to set a button near the TVS to ESD protection. The image below for reference circuit:

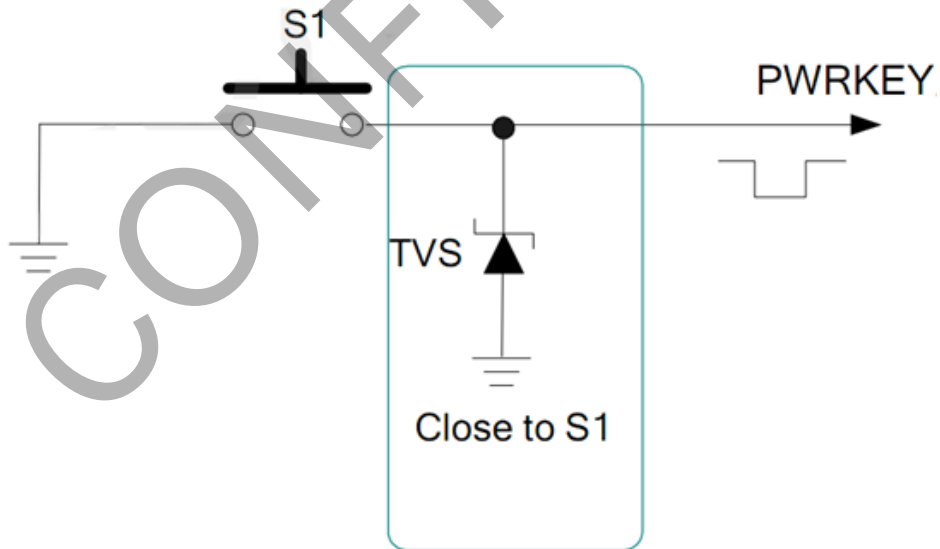


Figure 3-18: power on/off recommended circuit (physical buttons)

3.10 Interactive interface

3.10.1 Pin definition

Table 3-16 list the interface is mainly with the application processor interactive interface, including query, wake up, status indication, flight mode interface.

Table 3-16 Interactive interface

Pin No.	Signal	I/O type	Descriptions
46	WAKEUP_IN	DI	Default: GPIO Optional: Input pin as wake up interrupt signal to module from host.
47	WAKEUP_OUT	DO	Default: GPIO Optional: Output pin as the module wake up the AP
59	STATUS	DO	AP inquire the module status
48	FLGHTMODE	DI	Pull down this PIN made the system enter in flight mode, at this mode will tune off all the wireless function
42	MB_GPIO_0	DO	General GPIO module output (used for keyboard backlighting, etc.)

3.10.2 Interactive interface application

L510-3 provides three shook hands with application processor communication signals. Application processor can query whether the module boot normal work through STATUS. Through the WAKEUP_OUT query module is in sleep mode, and sleep in the module, through WAKEUP_IN wake module. Similarly, when application processor in the sleep state, the L510-3 modules can through WAKEUP_OUT wake application processor.

- STATUS: Module sleep instructions, high level indicator to sleep, low level instructions for the awakened state;
- WAKEUP_IN: The host can lower the signal awakens the module, If, low level has maintained, module can't sleep.

- WAKEUP_OUT: when L510-3 need to communicate with the AP, module can be set this pin for low level to awaken application processor.
- FLGHTMODE: Through the external input low level module into flight mode;

FLIGHTMODE pin can be used to control module to enter or exit the flight mode. In flight mode, L510-3 internal radio frequency circuit is closed. FLIGHTMODE reference circuit as shown in the figure below:

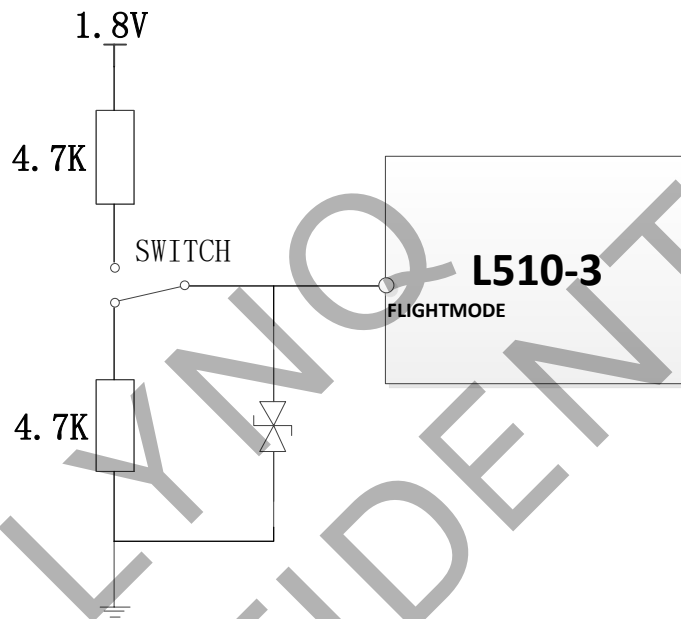


Figure 3-19: Flight mode recommended circuit (physical buttons)

3.11 Net Light interface

3.11.1 Pin define

Table 3-17 LED pin definitions

Pin No.	Net name	I/O type	description
39	NETLIGHT	DO	Module net state identify control LED port

3.11.2 Net light application

The L510-3 module has 1 pins for controlling the LED display, which can be used as an indicator of network connection status. Different network states are represented by the mode of the flashing light. This pin is an GPIO, with An external NPN Transistor, External connect VBAT can directly drive LED. Drive current capacity varies according to external NPN model, recommend use DTC143ZEBTL, Drive current biggest can reach 100 mA, below is the reference circuit.

Table 3-18 LED pin signal working status

Network modulation state	Module working condition
Normally on	Looking for the net, or on the line
200ms on / 200ms off	Data connection established
800ms on / 800ms off	Network registered
Long off	Shutdown, or sleep mode

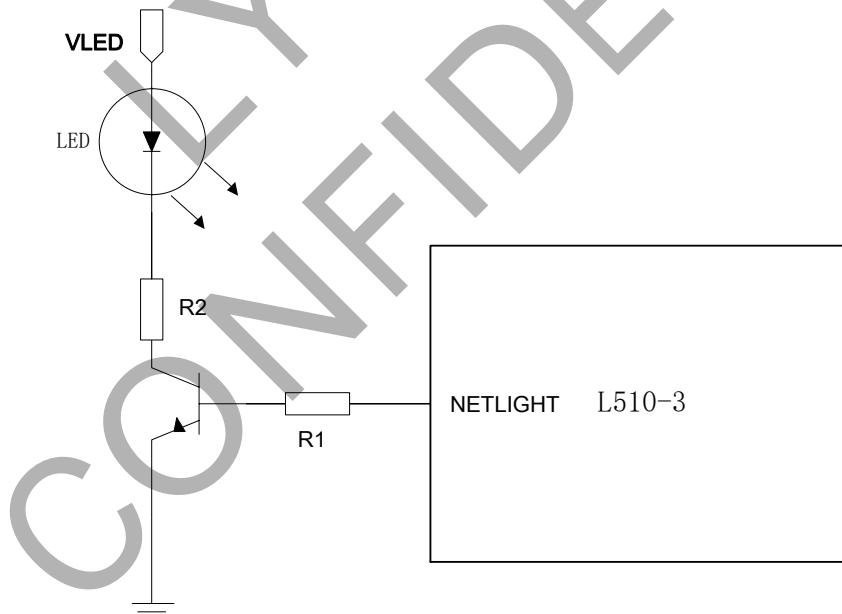


Figure 3-20 Status indicator reference circuit

Note: R1, R2 value according to the voltage VLED and LED working current.

Table 3-18 NETLIGHT status

Net Status	Module working status
Always on	Searching Network/Call Connect
200ms ON, 200ms OFF	Data Transmit
800ms ON, 800ms OFF	Registered network
OFF	Power off / Sleep

Note: NETLIGHT output low level as "ON", and high level as "OFF".

3.12 System boot configuration and download

3.12.1 Pin definition

Force module to enter USB download mode by pulling up the FORCE_USB_BOOT and pulling down the PWRKEY.

Table 3-19 Boot configuration and force USB download

Pin No.	Net name	Function description	note
58	GPIO(System on)	FORCE_USB_BOOT (before system on)	Multiplex pin

3.12.2 Boot configuration and force USB interface application

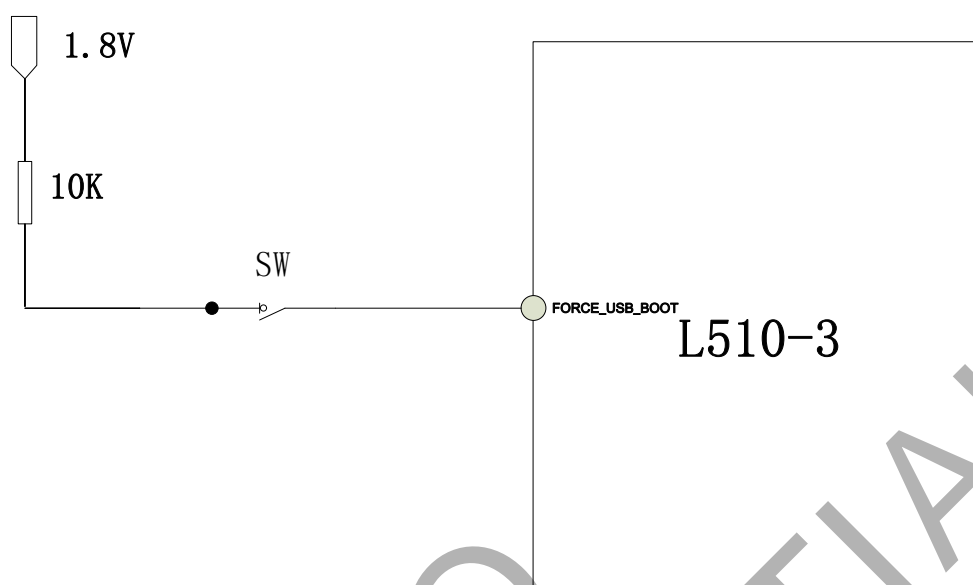


Figure 3-21 boot configuration and force USB download recommended circuit

3.13 Analog and Digital conversion (ADC) interface

L510-3 integrated two analog-to-digital conversion interface, specific parameters are as follows:

Table 3-20 ADC1 characters

characters	Min.	Typ.	Max.	Unit
ADC1 accuracy	-11	±6	11	mv
ADC1 Input voltage range	0		1.8	v
ADC1 Input resistance	1	--	--	MΩ
Transfer time	--	514	550	us

Note: The need for special software version to support access to the ADC.

3.14 I2C interface

I2C is used to communicate with peripheral equipment and can be operated as either a transmitter or receiver, depending on the device function. Both SDA and SCL are bidirectional lines connected with I2C interface. Its operation voltage is 1.8V. High speed mode transmission rate can reach 400 KBPS, Because L510-3 haven't internal pulled up to the I2C interface, so in your design need pull up. Below figure is the reference design:

I2C is used as the control interface for communication with perimeters. The operating voltage is 1.8V, and the transmission rate in high-speed mode can reach 1MHZ. There is a pull-up resistance inside the L510-3 module, We still recommend keeping the NC resistance pull-up Settings externally.

Below figure is the reference design:

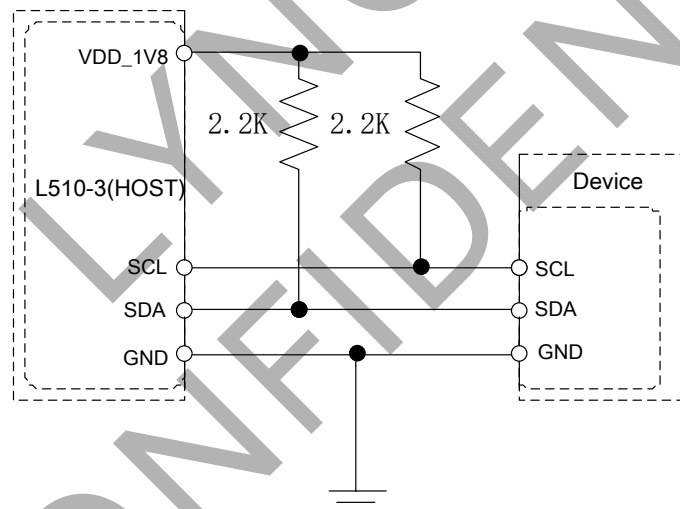


Figure 3-22 I2C reference design

Note: 1. L510-3 I2C only support host mode.

2. Only special software version support inquire the I2C.

3.15 SPI interface

SPI signal consists of four signal lines: CS, CLK, MOSI and MISO. When SPI signal is used as the main device, its maximum speed can reach 50MHZ; when SPI signal is used as a slave device, its maximum speed can reach 25MHZ. Below figure is the reference design:

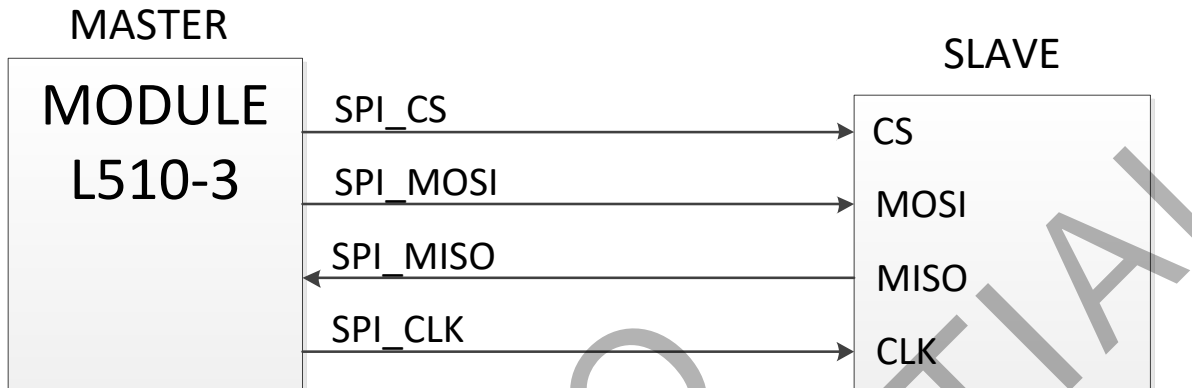


图 3-23 SPI MAIN DEVICE

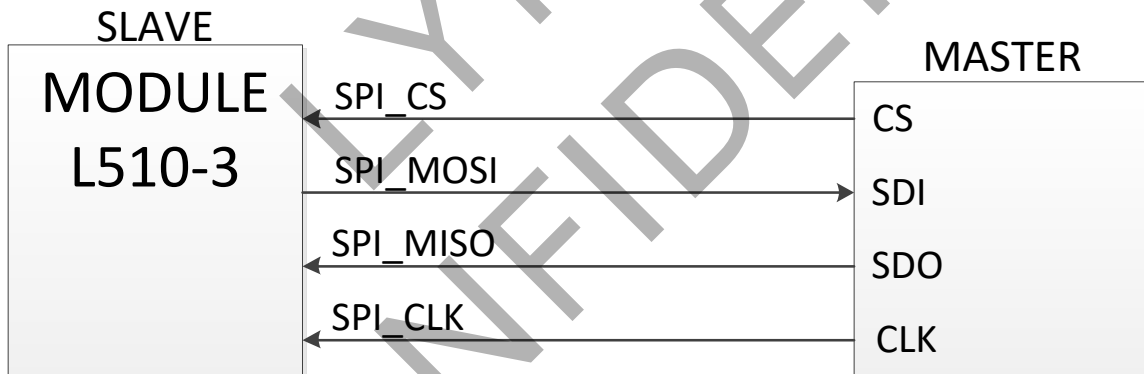


图 3-24 SPI SLAVE DEVICE

3.16 Antenna interface

3.16.1 RF signal PCB layout guide

L510-3 provides RF antenna interface. Customer's antenna should be located in the host board and

connected to module's antenna pad through micro-strip line or other types of RF trace and the trace impedance must be controlled in 50Ω. we recommends that the total insertion loss between the antenna pad and antenna should meet the following requirements:

- LTE (F<1GHz) <0.5dB
- LTE (1GHz<F<2GHz) <0.9dB
- LTE (2GHz<F) <1.2dB

To facilitate the antenna tuning and certification test, a RF connector and an antenna matching circuit should be added. The following figure is the recommended circuit.

The antenna feed point is defined as shown in below table:

Table 3-21 antenna pin definition

Pin No.	Signal	I/O Typ.	Description
18	MAIN_ANT	AI/AO	Module main antenna
21	GNSS_ANT	AI	GNSS Antenna

3.16.2 Applications

For convenience of antenna tuning and certification test, should increase RF connectors and the antenna matching circuit, below is a recommended circuit:

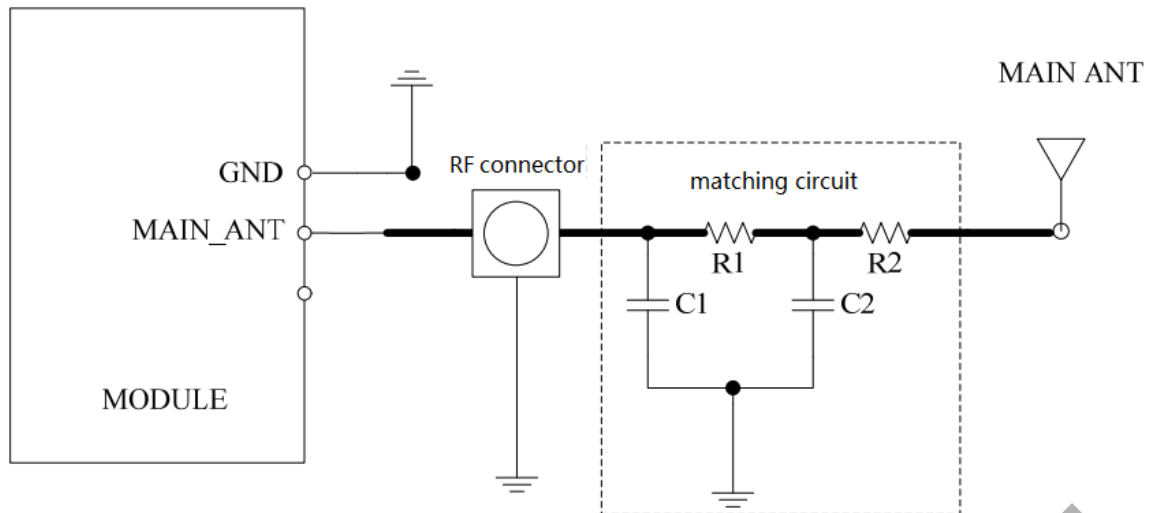


Figure 3-26 Main antenna matching circuit diagram (MAIN_ANT)

In this figure, the components R1, C1, C2 and R2 is used for antenna matching, the value of components can only be got after the antenna tuning, usually, they are provided by antenna vendor. By default, the R1, R2 are 0 Ohm resistors, and the C1, C2 are reserved for tuning.

The RF test connector in the figure is used for the conducted RF performance test, and should be placed as close as to the module's antenna pin. The traces impedance between components must be controlled in 50ohm.

If the environment is very static, you can add TVS or 100nH inductance to the antenna end to enhance the anti-static capability.

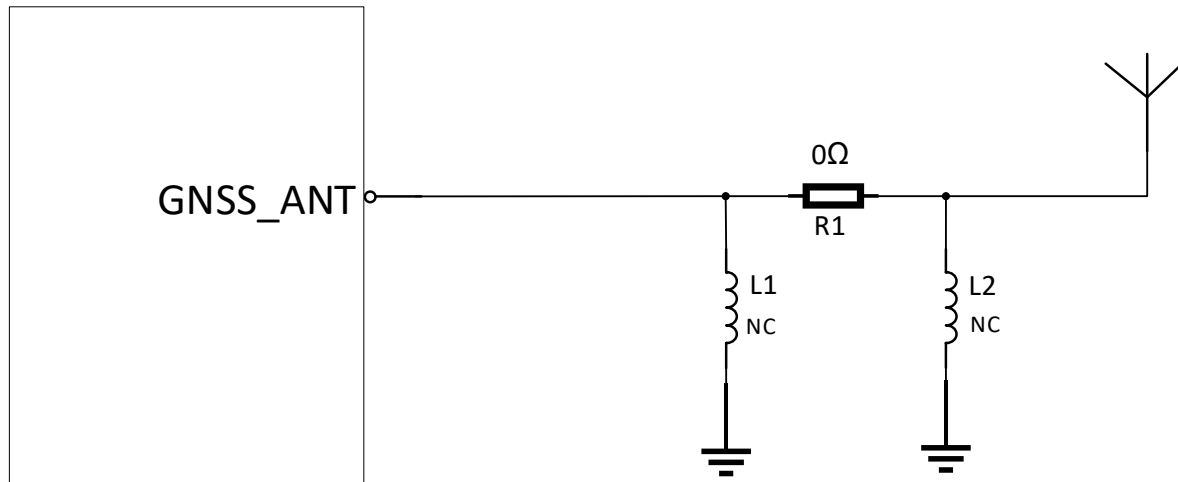


Figure 3-27 GNSS antenna matching circuit diagram

In this figure, the components R1, L1 and L2 is used for antenna matching, the value of components can only be got after the antenna tuning.

3.16.3 Antenna Layout guideline

In layout design, antenna RF transmission line must ensure the characteristic impedance = 50 ohm. The characteristic impedance depend on substrate board, line width and the distance from the ground plane. As shown in figure 3-20 is the layout of antenna feed point of reference for clearance area.

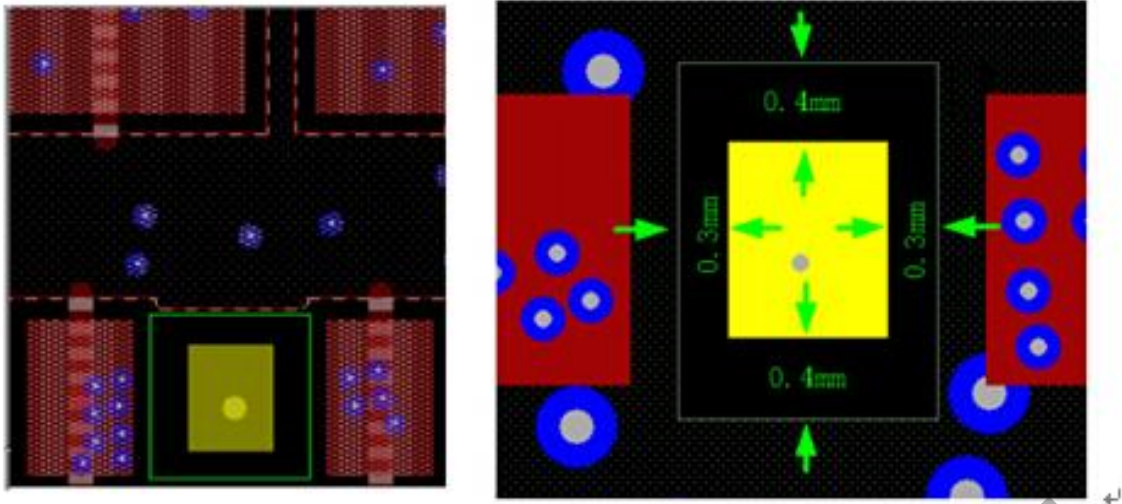


Figure 3-27 antenna feed point

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4. Product characteristics

4.1 Absolute parameters

The following table shows the state of the absolute maximum work in abnormal situation. Exceed the limit value will likely result in permanent damage to the module.

Table 4-1 L510-3 absolute parameters

Parameter	Min.	Max.	Unit
VBAT absolute voltage parameter	-0.5	6.0	V
USB_VBUS absolute voltage parameter	-0.5	5.25	V
I/O absolute voltage parameter: PWRKEY, RESET, SPI, GPIO, I2C, PCM, UART, SD1_DET, USIM_DET	-0.3	2.1	V

4.2 Operation condition

4.2.1 Operation voltage

This product is a DC input voltage range of 3.4 V to 4.2 V, the typical value of 3.8 V, as shown in below table.

Table 4-2 Input DC voltage

Parameter	Min.	Typ.	Max.	Unit
VBAT Voltage	3.3	3.8	4.5	V
USB_VBUS Voltage	4.0	5.0	5.25	V

Note: About L510-3 dc electric property, please refer to part 3.3 digital I/O characteristics.

4.2.2 Work mode

Table 4-3 work mode

Mode		Description
Normal operation mode	(LTE) Sleep	In this case, the current consumption of module will be reduced to the minimal level. In sleep mode, the module can still receive paging message and SMS.
	(LTE) Idle	Software is active. Module is registered to the LTE network, and the module is ready to communicate.
	(LTE) talking	Connection between two subscribers is in progress. In this case, the power consumption depends on network settings such as DTX off/on, FR/EFR/HR, hopping sequences, antenna.
	(LTE) Standby	Module is ready for GPRS/EDGE/WCDMA/TD-SCDMA/EVDO/LTE data transfer, but no data is currently sent or received. In this case, power consumption depends on network settings and EDGE/HSPA+ /LTE configuration.
	(LTE) Data transfer	There is GPRS/EDGE/WCDMA/TD-SCDMA/EVDO/LTE data transfer in progress. In this case, power consumption is related to network settings (e.g. power control level); uplink/downlink data rates and GPRS configuration (e.g. used multi-slot settings).
Minimum mode	AT command "AT+CFUN" can be used to set the module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the module will not work or the USIM card will not be accessible, or both RF part and USIM card will be closed, and the serial port is still accessible. The power consumption in this mode is lower than normal mode.	
Flight mode	Use the "AT + CFUN = 7" command or lower FLIGHTMODE pins, the module can be configured to flight mode under without removing the power supply condition. In this case, the RF part does not work, but still can use the serial port and USB, the power consumption is lower than normal working mode.	

Power off	Through the "AT + CPOF" command or lower PWRKEY pin can power off L510-3. At this mode, the module of internal power supply will be closed, and the system is stop running also. The UART and USB are unavailable.
Sleep mode	In sleep mode, the module power consumption to a minimum, but the module is still able to receive paging information and SMS.
PSM (Power Saving mode)	The "AT +CPSMS= 1" command allows the module to enter the Power Saving mode to get the module into ultra-low-power mode. In this mode, the module will disable all functions except the RTC system clock, and cannot accept the network message; Lower PWRKEY in PSM mode can force the module to exit PSM mode.

4.2.3 Current consumption

The power consumption in suspended mode and without USB connection is listed in the table below.

Table 4-4 L510-3_G working current consumption (VBAT=3.8V)

Power off	
Power off current	TBD
PSM	TBD
Sleep/Idle	
GSM	Sleep mode typical: TBD Idle mode typical: TBD
LTE Data transmission	
B1	@1.4Mbps typical: TBD
B3	@1.4Mbps typical: TBD
B7	@1.4Mbps typical: TBD
B8	@1.4Mbps typical: TBD
B20	@1.4Mbps typical: TBD

B28

@1.4Mbps typical: TBD

4.3 Working and storage temperature

The operating temperature and storage temperature of L510-3 is listed in the following table.

Table 4-6 Operating temperature

Parameter	Min.	Typ.	Max.	Unit
Extended operation temperature*	-40	25	85	°C
Storage temperature	-45	25	90	°C

*Note: Module is able to make and receive voice calls, data calls, SMS and make

GPRS/WCDMA/HSPA+/LTE traffic in -40°C ~ +85°C. Temperatures outside of the range -30°C ~ +80°C might slightly deviate from ETSI specifications.

4.4 ESD performance

L510-3 is electrostatic sensitive device, therefore, the user in the production, assembly and operation of the module must pay attention to the electrostatic protection. L510-3 ESD performance parameters in the following table:

Table 4-7 ESD performance parameters (temperature 25 °C, humidity: 45%)

Net	contact	air
VBAT GND	±4KV	±8KV
Antenna port	±4KV	±8KV
UART	±4KV	±8KV
USB	±4KV	±8KV

Other PADS	$\pm 4KV$	$\pm 8KV$
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5. Design guideline

This chapter provides a general design of the products instruction, the user can refer to design guidance for design, make products to achieve better performance.

5.1 General design rules and requirements

Users in the design of this product is peripheral circuit, the first to ensure the external power supply circuit can provide enough power supply capacity, And the requirements for high speed signal lines USB control 90 ohm + / - 10% difference impedance. For general signal interface, require the user to us in strict accordance with the requirements of design, in line with the interface signal level matching, in case the level of damage to the module. This product its own radio frequency index is good, customers need to design in accordance with the requirements the mainboard side antenna circuit and corresponding impedance control, otherwise it will affect the whole RF index.

5.2 Reference circuit

Overall reference circuit design please refer 《L510-3 reference design》 .

5.3 RF part design guideline

Early antenna design considerations

- **Pre-project evaluation**

The selection of the antenna position must first ensure that the antenna and the base station are kept in the horizontal direction, this produces the highest efficiency; Secondly, try to avoid placing the switch in the power supply or data line, chip and other devices or chips that produce electromagnetic interference. At the same time, the position of the hand can be avoided, so as to prevent the human body to produce attenuation; But also to reduce the radiation and the structure of the realization of the

need to take into account. So, At the beginning of the design need to structure, ID, circuit, antenna engineers together to evaluate the layout.

- **Antenna matching circuit**

If the module's radio frequency port and the antenna interface need to be transferred, the main board circuit design, The design of microstrip line or strip line between the module RF test base and the antenna interface between the microstrip line or the strip line by characteristic impedance 50 ohm, at the same time, reserved double L type matching circuit; If the antenna's RF connector can be directly stuck in the module's RF test base, can save the module of the RF port and the antenna interface between the transfer.

5.4 EMC and ESD design advice

Users should take full account of the EMC problem caused by signal integrity and power integrity in the design of the whole machine, In the module of the peripheral circuit layout, for power and signal lines, etc., to maintain the spacing of 2 times line width. Can effectively reduce the coupling between the signal, so that the signal has a clean, the return path. When the peripheral power supply circuit is designed, the decoupling capacitor should be placed close to the module power supply pin, High frequency high speed circuit and sensitive circuit should be far from the edge of PCB, and the layout of the layout as far as possible to reduce the interference between each other, and the sensitive signal is protected. The circuit or device that may interfere with the operation of the system board is designed.

This product is embedded in the system board side, design, need to pay attention to the ESD protection, the key input and output signal interface, such as (U) SIM card interface need to be placed close to the protection of ESD devices. In addition to the

motherboard side, the user is required to design the structure and PCB layout, ensure that the metal shield is fully grounded, and set up an unobstructed discharge passage for the electrostatic discharge.

6. Manufacturers

6.1 Steel mesh design

- At the bottom of the module pad thermal, can be reduced by way of steel mesh

openings, reduce the risk of short circuit between the thermal and the module of the module Pin, have certain effect;

- Module pad thermal welded steel mesh openings are recommended for reference. Figure 6-1 is recommended for steel mesh and size.

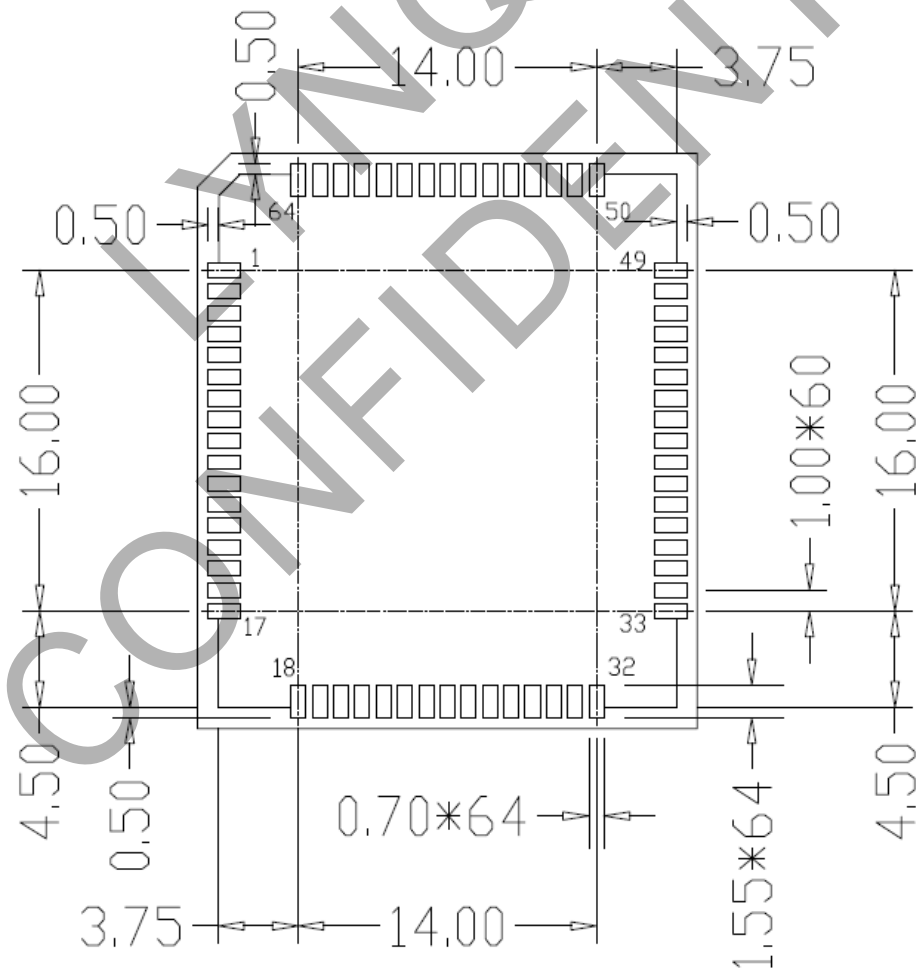


Figure 6-1 Steel mesh (unit mm)(detail A)

Note: The direction mark point only for identify the pin 1 position, should not embody in the steel mesh file.

6.2 Temperature curve

In order to ensure soldering quality, special attention should be paid to the control of temperature curve pipes. The soldering profile shown below is only a general recommendation and should be adjusted according to the specific application and manufacturing.

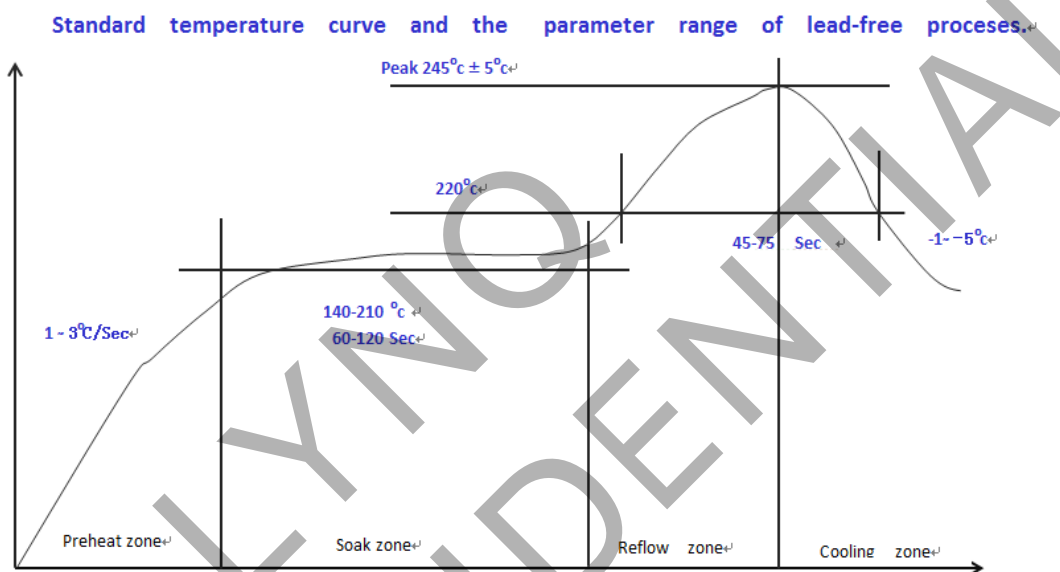


Figure 6-2 The reference temperature curve

6.3 Device moisture-sensitivity level (MSL)

L510-3 module complies with the humidity level 3. At a temperature of <30 degrees and relative humidity of $<60\%$ of the environmental conditions, dry pack to perform J-STD-020C specification according to IPC / JEDEC standard. At a temperature of <40 degrees and a relative humidity of $<90\%$ of the environmental conditions, in the case of unopened shelf life of 12 months. After unpacking, Table6-1 shows the module shelf life at different times corresponding to the level of humidity.

Table 6-2 Moisture sensitivity level and floor life

Rank	Factory Environment: $23 \pm 5^{\circ}\text{C}$, Relative humidity $< 60\% \text{RH}$
1 RH $^{\circ}\text{C}$	Indefinite Shelf Life in the environment $\leq +30^{\circ}\text{C}/85\% \text{RH}$ Conditions
2	1 Year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.

After unpacking, < 30 degrees in temperature and relative humidity $< 60\%$ environmental conditions, 168 hours in the SMT patch. If not meet the above conditions need to be baked.

NOTES: For product handling, storage, processing, IPC / JEDEC J-STD-020C must be followed

6.4 Baking Requirements

Due to the humidity sensitive characteristics of the L510-3 module, the L510-3 is a vacuum packaging, which can be stored for 12 months without damage to the package, and the ambient temperature is less than 40°C and the relative humidity is less than 90% . To meet one of the following conditions, the process of reflow soldering should be performed before the full bake (if trays are used, please note whether the tray is heat-resistant.), or the module may cause permanent damage to the process.

- 1、 Vacuum packing damage or leakage
- 2、 The module is exposed in the air for 168 hours or more
- 3、 The module is exposed in air for 168 hours, not meet the temperature < 30 degrees and relative humidity of the environment conditions $< 60\%$

Table 6-3 Baking requirements

Baking conditions	125°C±5°C RH	45°C±5°C RH
Baking time	8 hours	182 hours
Instructions	Do not use original pallet	Can use the original pallet

Note: The original packaging of the module cannot bear the high temperature of baking. The packaging needs to be removed before baking, otherwise the packaging will be damaged.

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7. Package Storage information

7.1 Package information

7.1.1 Tape and reel information

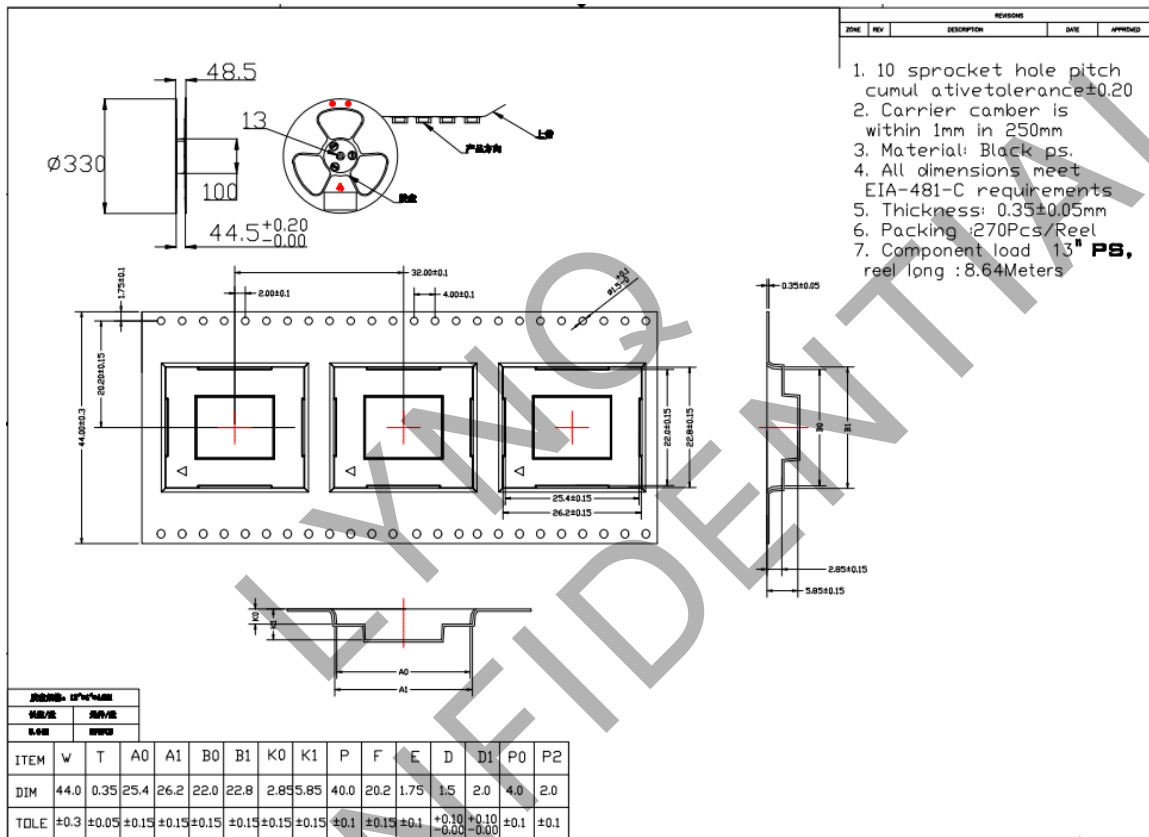


Figure 7-1 Tap and reel information

7.1.2 Package information

L510-3 packing diagram is as follows, every 4 volumes of material packed in a case between each volume of material has a bubble mat do isolation protection. Specific as shown in the figure below:

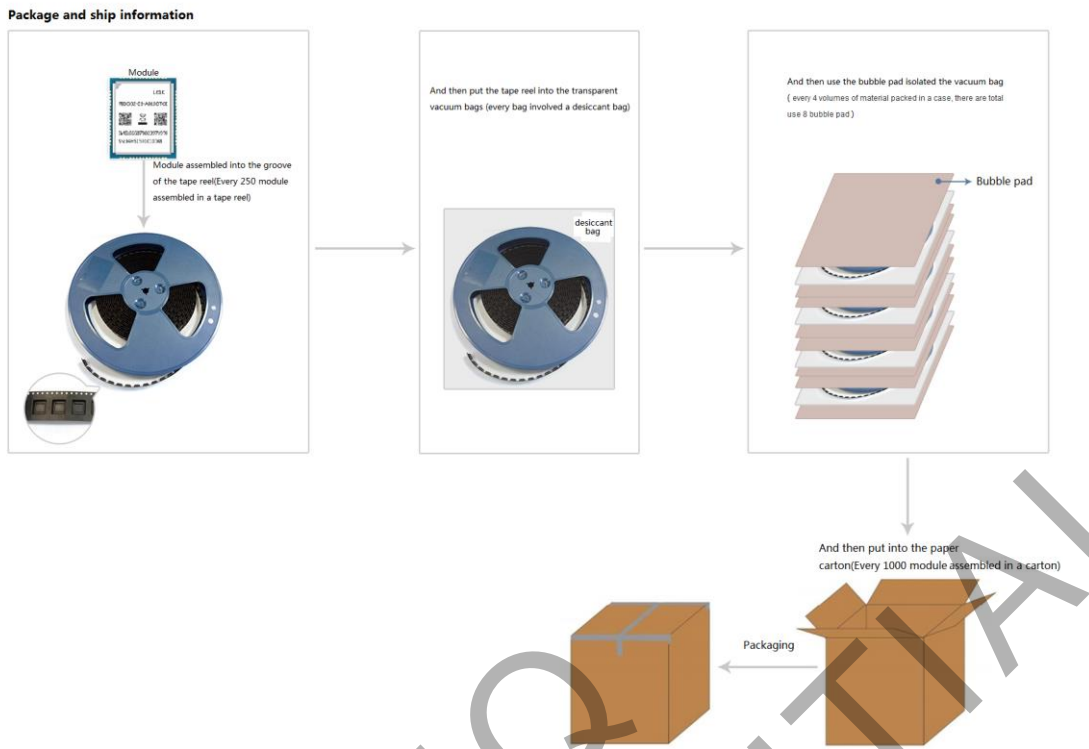


Figure 7-2 Package and ship information

7.2 Bagged storage conditions

L510-3 shipments in the form of vacuum sealing anti-static bag. Module of storage need to follow the following conditions: Environment below 40 Degrees Celsius temperature, air humidity is less than 90% of cases, the module can be in vacuum sealed bags for 12 months. Conditions set the storage environment Suggestions with reference to the following form.

Table 7-1 Storage conditions (less than 90% humidity of the air vacuum sealed packaging)

Parameter	Min.	Typ.	Max.	Unit
Storage temperature	-45	25	90	°C

When on the vacuum bags, if meet the following conditions, the module can be directly for reflow soldering (furnace temperature setting reference 6.2 furnace temperature curve) or other high

8. Safety Information

For the reasonable usage of the module, please comply with all these safety notices of this page. The product manufacturers should send followed safety information to user, operator or product's spec.



The devices using the module may disturb some electronic equipment. Put the module away from the phone, TV, radio and automation equipment to avoid the module and the equipment to interfere with each other.



Shut down the mobile device or change to flying mode before boarding. The Using of wireless appliances in an aircraft is forbidden to avoid the interference, or else cause to unsafe flying, even violate the law.



In hospital or health care center, switch off the mobile devices. RF interference may damage the medical devices, like hearing-aid, cochlear implant and heart pacemaker etc.



Mobile devices can't guarantee to connect in all conditions, like no fee or with an invalid SIM card. When you need emergent help, please remember using emergency calls and make sure your device power on in an area with well signal.



Put the module away from inflammable gases. Switch off the mobile device when close to gas station, oil depot, chemical plant etc.

