

### FEATURES

- Double Side Cooling
- High Surge Capability

### APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

### VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ V	Conditions
DCR3640W52*	5200	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 300\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ , $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR3640W50	5000	
DCR3640W48	4800	
DCR3640W46	4600	

Lower voltage grades available.  
 5000V @  $-40^{\circ}\text{C}$ , 5200V @  $0^{\circ}\text{C}$

### ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

### DCR3640W52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### KEY PARAMETERS

$V_{DRM}$	<b>5200V</b>
$I_{T(AV)}$	<b>3550A</b>
$I_{TSM}$	<b>49000A</b>
$dV/dt^*$	<b>1500V/<math>\mu\text{s}</math></b>
$dI/dt$	<b>400A/<math>\mu\text{s}</math></b>

\* Higher  $dV/dt$  selections available

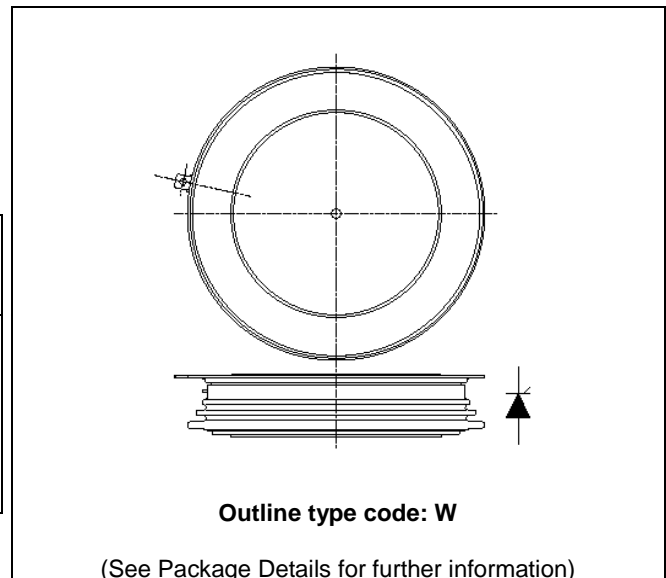


Fig. 1 Package outline

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3550	A
$I_{T(RMS)}$	RMS value	-	5576	A
$I_T$	Continuous (direct) on-state current	-	5240	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	49	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	12.0	$\text{MA}^2\text{s}$

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00631	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.01115	$^{\circ}\text{C/W}$
			Cathode DC	-	0.01453	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 76kN (with mounting compound)	Double side	-	0.0014	$^{\circ}\text{C/W}$
			Single side	-	0.0028	$^{\circ}\text{C/W}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}\text{C}$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}\text{C}$	
$F_m$	Clamping force		68.0	84.0	kN	

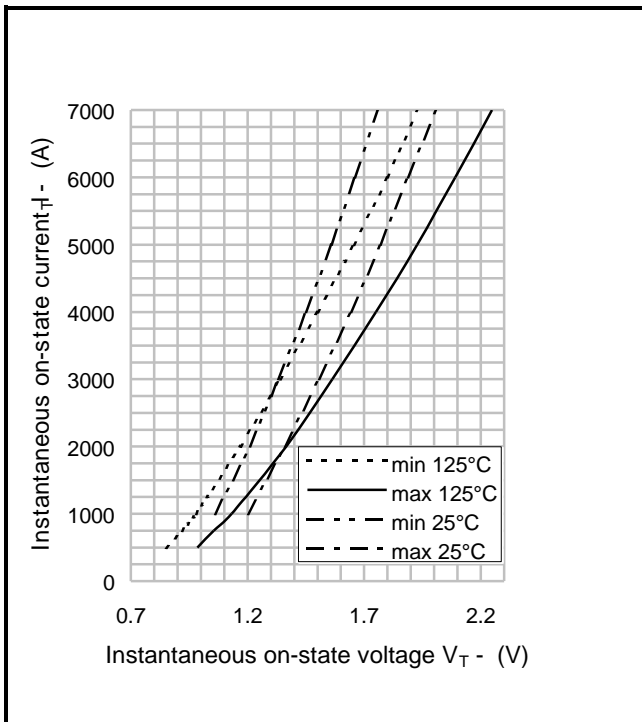
**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_{case} = 125^{\circ}C$	-	300	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^{\circ}C$ , gate open	-	1500	V/ $\mu s$	
dI/dt	Rate of rise of on-state current	From 67% $V_{DRM}$ to $2x I_{T(AV)}$	Repetitive 50Hz	-	200	A/ $\mu s$
		Gate source 30V, 10 $\Omega$ , $t_r < 0.5\mu s$ , $T_j = 125^{\circ}C$	Non-repetitive	-	400	A/ $\mu s$
$V_{T(TO)}$	Threshold voltage – Low level	500A to 1700A at $T_{case} = 125^{\circ}C$	-	0.86	V	
	Threshold voltage – High level	1700A to 5000A at $T_{case} = 125^{\circ}C$	-	0.98	V	
$r_T$	On-state slope resistance – Low level	500A to 1700A at $T_{case} = 125^{\circ}C$	-	0.2533	m $\Omega$	
	On-state slope resistance – High level	1700A to 5000A at $T_{case} = 125^{\circ}C$	-	0.1886	m $\Omega$	
$t_{gd}$	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, 10 $\Omega$ $t_r = 0.5\mu s$ , $T_j = 25^{\circ}C$	-	3	$\mu s$	
$t_q$	Turn-off time	$T_j = 125^{\circ}C$ , $V_R = 200V$ , dI/dt = 1A/ $\mu s$ , dV <sub>DR</sub> /dt = 20V/ $\mu s$ linear	400	750	$\mu s$	
$Q_S$	Stored charge	$I_T = 2000A$ , $T_j = 125^{\circ}C$ , dI/dt – 1A/ $\mu s$ ,	2700	6325	$\mu C$	
$I_L$	Latching current	$T_j = 25^{\circ}C$ , $V_D = 5V$	-	3	A	
$I_H$	Holding current	$T_j = 25^{\circ}C$ , $R_{G-K} = \infty$ , $I_{TM} = 500A$ , $I_T = 5A$	-	300	mA	

**GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	400	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	15	mA

**CURVES**



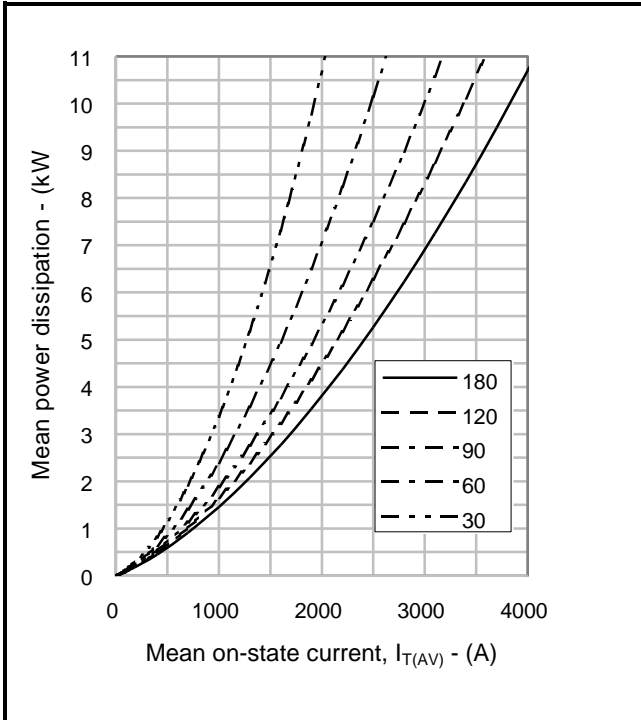
**Fig.2 Maximum & minimum on-state characteristics**

**V<sub>TM</sub> EQUATION**

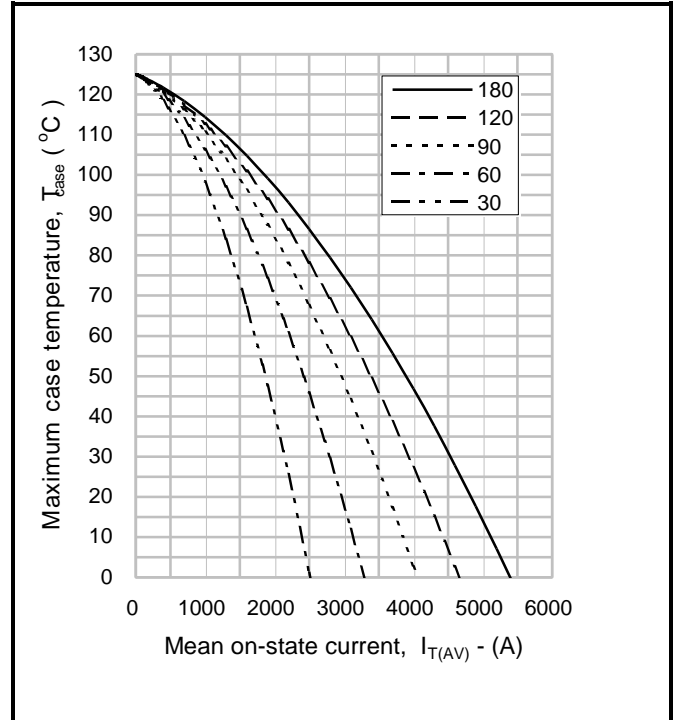
$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.722818  
 B = - 0.002455  
 C = 0.000096  
 D = 0.010486

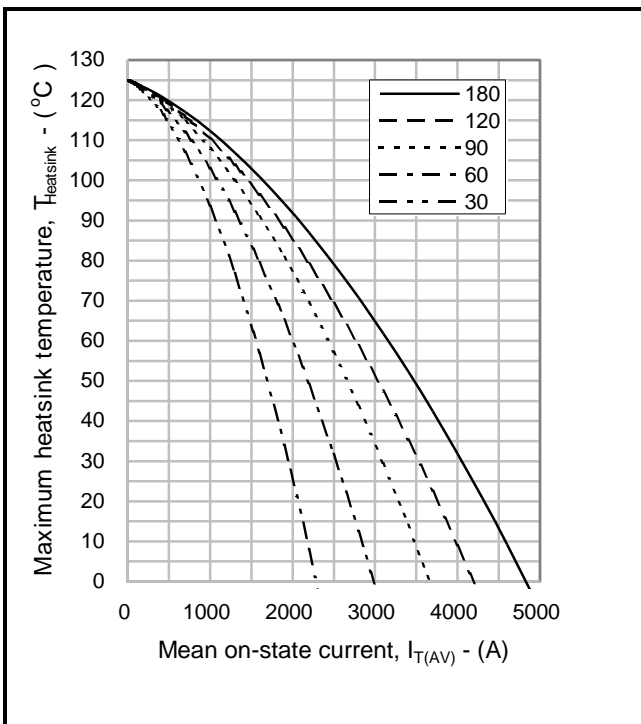
these values are valid for T<sub>j</sub> = 125°C for I<sub>T</sub> 100A to 7000A



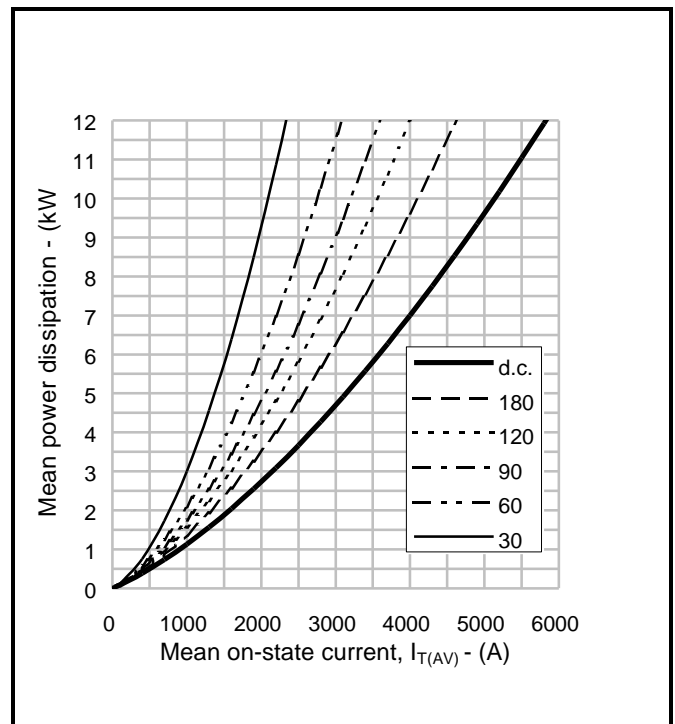
**Fig.3 On-state power dissipation – sine wave**



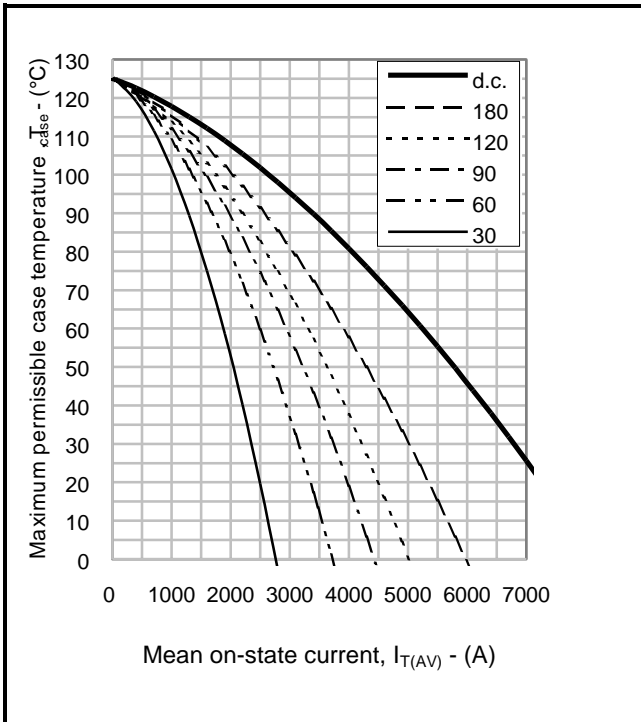
**Fig.4 Maximum permissible case temperature, double side cooled – sine wave**



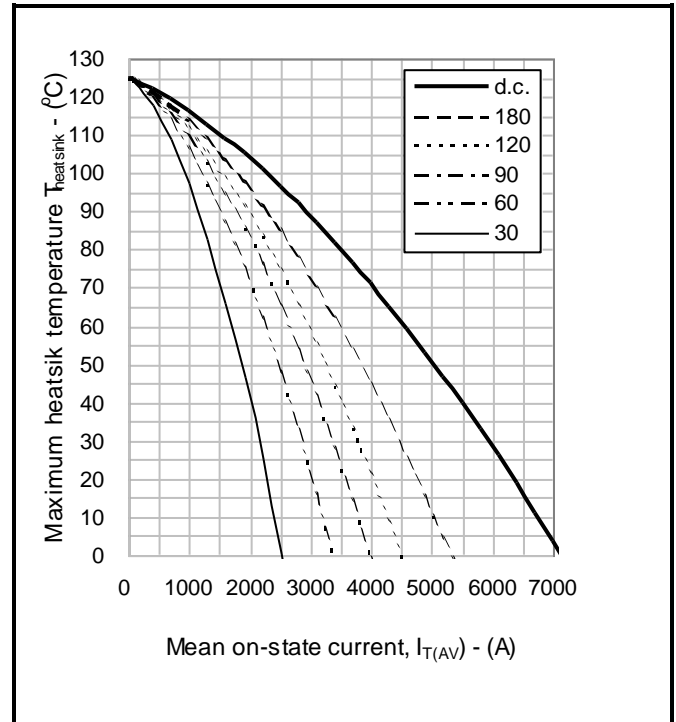
**Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave**



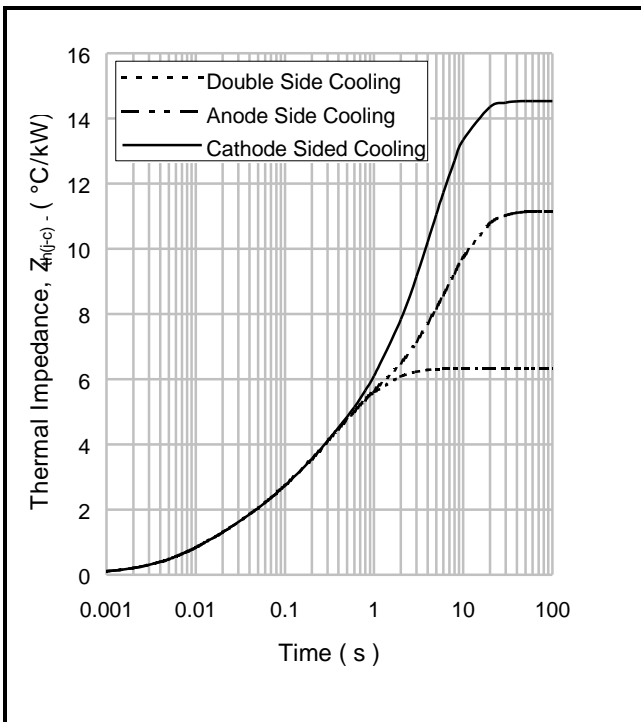
**Fig.6 On-state power dissipation – rectangular wave**



**Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave**



**Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave**



**Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)**

		1	2	3	4
Double side cooled	$R_{\theta}$ (°C/kW)	0.8816	1.2993	2.8048	1.3305
	$T_1$ (s)	0.0106818	0.058404	0.3584979	1.1285
Anode side cooled	$R_{\theta}$ (°C/kW)	1.5197	3.2398	5.7622	0.6312
	$T_1$ (s)	0.0170581	0.2424644	6.013	15.364
Cathode side cooled	$R_{\theta}$ (°C/kW)	1.4106	2.4667	6.7451	3.9054
	$T_1$ (s)	0.0158344	0.1786951	3.6201	6.196

$$Z_{th} = \sum [R_i \times (1 - \exp. -(t/t_i))] \quad [1]$$

$\Delta R_{th(j-c)}$  Conduction

Tables show the increments of thermal resistance  $R_{th(j-c)}$  when the device operates at conduction angles other than d.c.

Double side cooling		
$\eta^\circ$	$\Delta Z_{th} (z)$	
	sine.	rect.
180	1.00	0.67
120	1.16	0.97
90	1.33	1.13
60	1.48	1.31
30	1.61	1.51
15	1.66	1.61

Anode Side Cooling		
$\eta^\circ$	$\Delta Z_{th} (z)$	
	sine.	rect.
180	0.94	0.64
120	1.08	0.91
90	1.23	1.06
60	1.37	1.22
30	1.47	1.38
15	1.52	1.47

Cathode Sided Cooling		
$\eta^\circ$	$\Delta Z_{th} (z)$	
	sine.	rect.
180	0.95	0.65
120	1.09	0.92
90	1.25	1.07
60	1.38	1.23
30	1.49	1.40
15	1.54	1.49

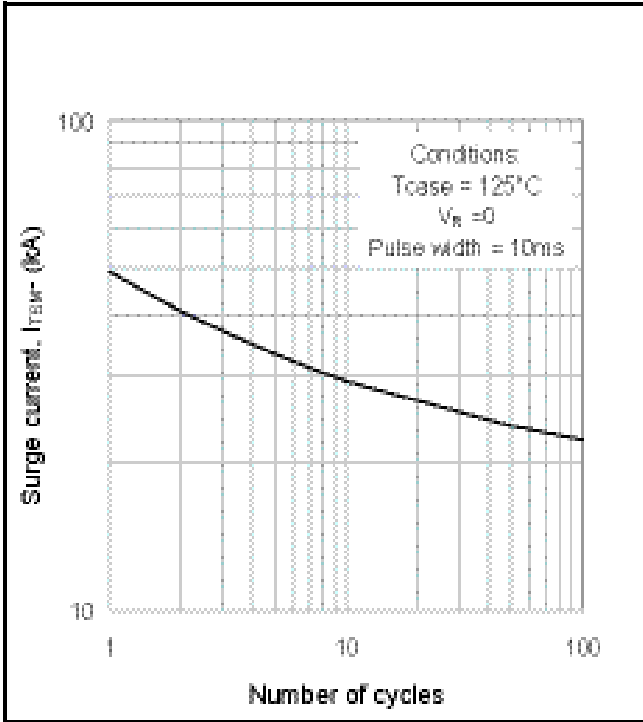


Fig.10 Multi-cycle surge current

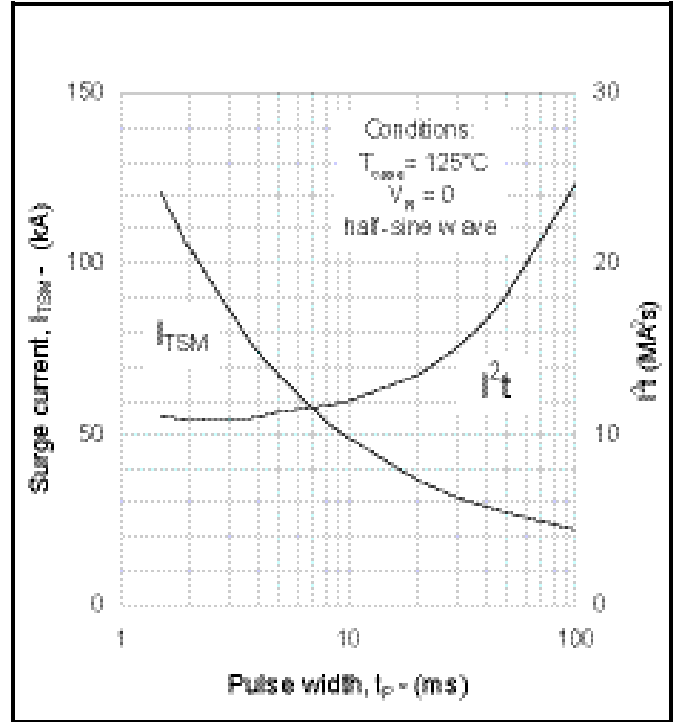


Fig.11 Single-cycle surge current

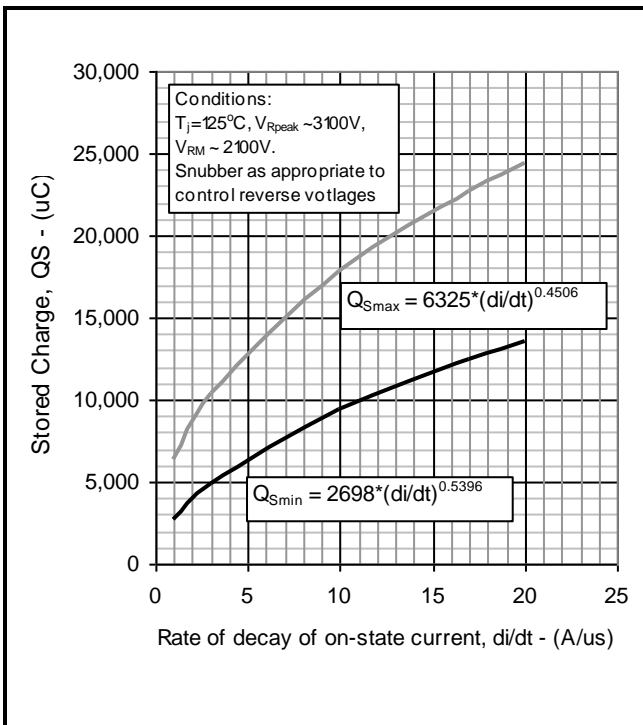


Fig.12 Stored Charge

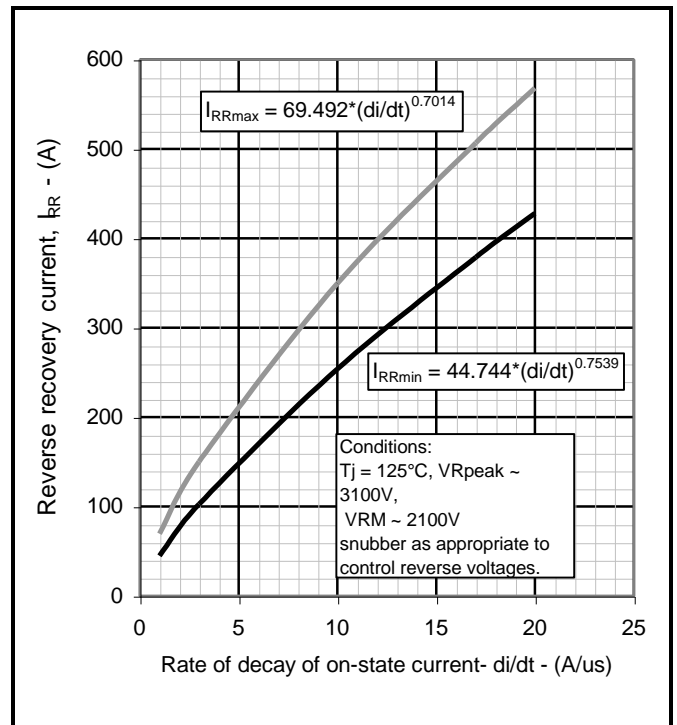


Fig.13 Reverse recovery current

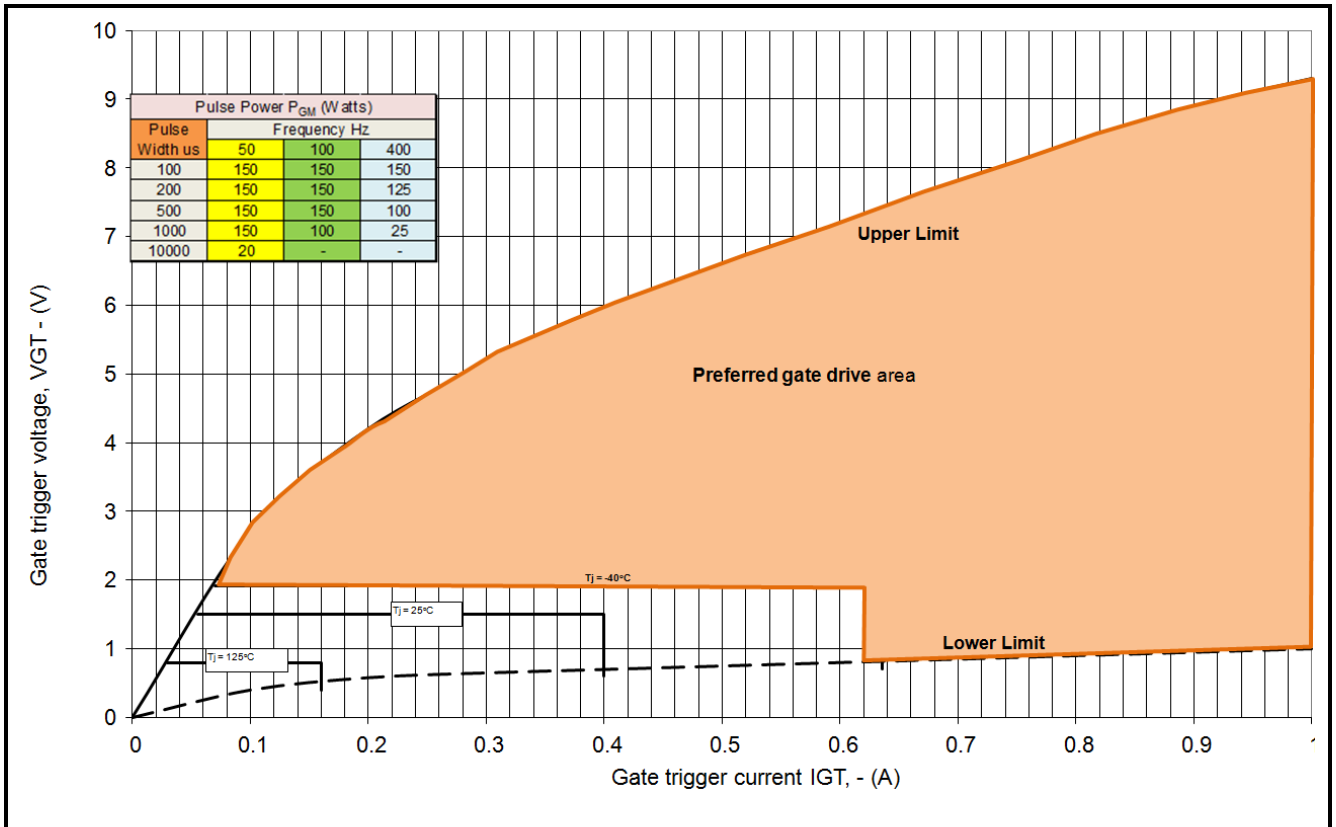


Fig14 Gate Characteristics

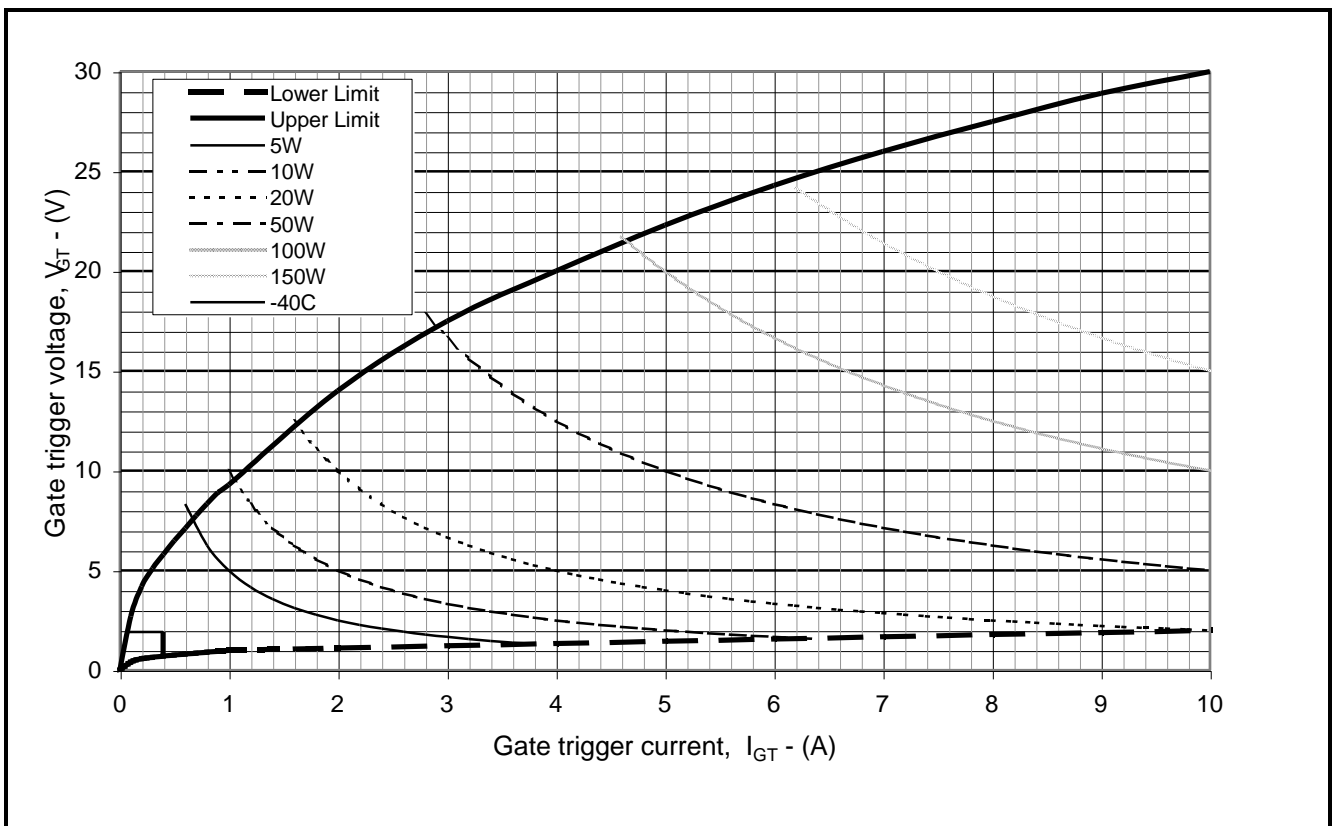
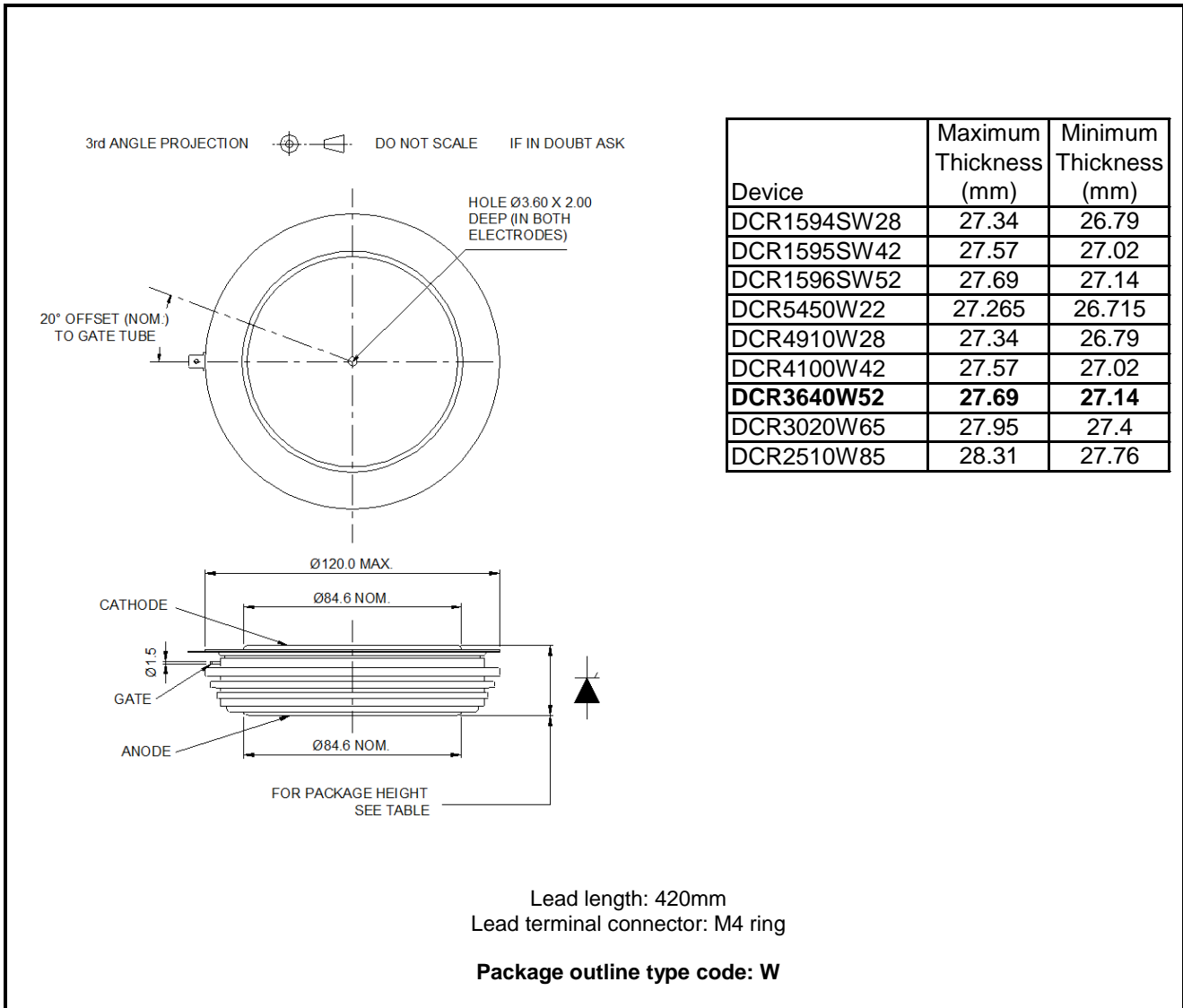


Fig. 15 Gate characteristics



**PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



**Fig.16 Package outline**

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