



Phase Control Thyristor Preliminary Information

DS5746-3.5 January 2009 (LN 26573)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

| Part and Ordering Number | Repetitive Peak Voltages V_{DRM} and V_{RRM} V | Conditions |
|--------------------------|---|---|
| DCR2400B85* | 8500 | $T_{vj} = -40^{\circ}\text{C}$ to 125°C , $I_{DRM} = I_{RRM} = 300\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, V_{DSM} & $V_{RSM} =$ V_{DRM} & $V_{RRM} + 100\text{V}$ respectively |
| DCR2400B80 | 8000 | |
| DCR2400B75 | 7500 | |
| DCR2400B70 | 7000 | |

Lower voltage grades available.
 *8200V @ -40°C , 8500V @ 0°C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR2400B85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

| | |
|-------------|----------------------|
| V_{DRM} | 8500V |
| $I_{T(AV)}$ | 2370A |
| I_{TSM} | 32500A |
| dV/dt^* | 1500V/ μs |
| di/dt | 300A/ μs |

* Higher dV/dt selections available

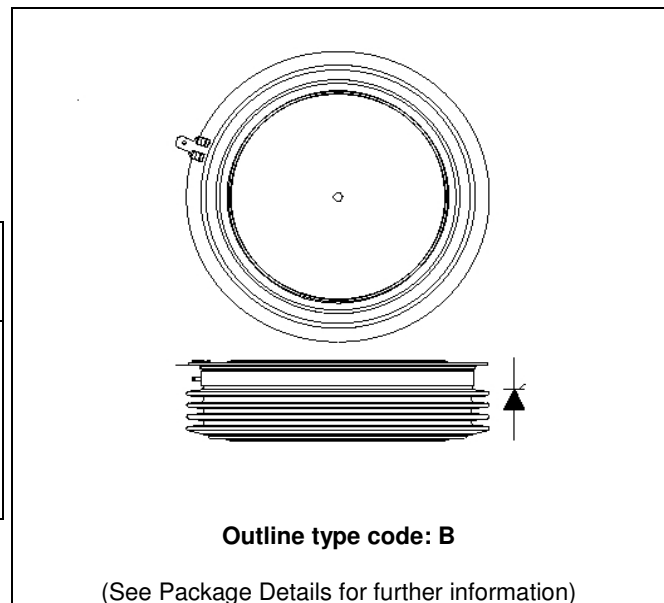


Fig. 1 Package outline

CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$ unless stated otherwise

| Symbol | Parameter | Test Conditions | Max. | Units |
|---------------------------|--------------------------------------|--------------------------|------|-------|
| Double Side Cooled | | | | |
| $I_{T(AV)}$ | Mean on-state current | Half wave resistive load | 2370 | A |
| $I_{T(RMS)}$ | RMS value | - | 3723 | A |
| I_T | Continuous (direct) on-state current | - | 3500 | A |

SURGE RATINGS

| Symbol | Parameter | Test Conditions | Max. | Units |
|-----------|---|--|------|-----------------------|
| I_{TSM} | Surge (non-repetitive) on-state current | 10ms half sine, $T_{case} = 125^{\circ}\text{C}$ | 32.5 | kA |
| I^2t | I^2t for fusing | $V_R = 0$ | 5.28 | MA^2s |

THERMAL AND MECHANICAL RATINGS

| Symbol | Parameter | Test Conditions | Min. | Max. | Units | |
|---------------|---------------------------------------|---|-------------|------|--------------------|----------------------|
| $R_{th(j-c)}$ | Thermal resistance – junction to case | Double side cooled | DC | - | 0.007 | $^{\circ}\text{C/W}$ |
| | | Single side cooled | Anode DC | - | 0.0116 | $^{\circ}\text{C/W}$ |
| | | | Cathode DC | - | 0.0181 | $^{\circ}\text{C/W}$ |
| $R_{th(c-h)}$ | Thermal resistance – case to heatsink | Clamping force 76.0kN (with mounting compound) | Double side | - | 0.0014 | $^{\circ}\text{C/W}$ |
| | | | Single side | - | 0.0028 | $^{\circ}\text{C/W}$ |
| T_{vj} | Virtual junction temperature | On-state (conducting) | - | 135 | $^{\circ}\text{C}$ | |
| | | Reverse (blocking) | - | 125 | $^{\circ}\text{C}$ | |
| T_{stg} | Storage temperature range | | -55 | 125 | $^{\circ}\text{C}$ | |
| F_m | Clamping force | | 68.0 | 84.0 | kN | |

DYNAMIC CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Min. | Max. | Units | |
|-------------------|---|---|-----------------|-------|------------|------------|
| I_{RRM}/I_{DRM} | Peak reverse and off-state current | At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$ | - | 300 | mA | |
| dV/dt | Max. linear rate of rise of off-state voltage | To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open | - | 1500 | V/ μs | |
| dI/dt | Rate of rise of on-state current | From 67% V_{DRM} to $2x I_{T(AV)}$ | Repetitive 50Hz | - | 150 | A/ μs |
| | | Gate source 30V, 10 Ω , $t_r < 0.5\mu s$, $T_j = 125^{\circ}C$ | Non-repetitive | - | 300 | A/ μs |
| $V_{T(TO)}$ | Threshold voltage – Low level | 500 to 2400A at $T_{case} = 125^{\circ}C$ | - | 1.037 | V | |
| | Threshold voltage – High level | 2400 to 72000A at $T_{case} = 125^{\circ}C$ | - | 1.229 | V | |
| r_T | On-state slope resistance – Low level | 500A to 2400A at $T_{case} = 125^{\circ}C$ | - | 0.487 | m Ω | |
| | On-state slope resistance – High level | 2400A to 72000A at $T_{case} = 125^{\circ}C$ | - | 0.398 | m Ω | |
| t_{gd} | Delay time | $V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu s$, $T_j = 25^{\circ}C$ | - | 3 | μs | |
| t_q | Turn-off time | $T_j = 125^{\circ}C$, $V_R = 200V$, $dI/dt = 1A/\mu s$, $dV_{DR}/dt = 20V/\mu s$ linear | 600 | 1000 | μs | |
| Q_S | Stored charge | $I_T = 2000A$, $T_j = 125^{\circ}C$, $dI/dt = 1A/\mu s$, | 6200 | 9000 | μC | |
| I_L | Latching current | $T_j = 25^{\circ}C$, $V_D = 5V$ | - | 3 | A | |
| I_H | Holding current | $T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$ | - | 300 | mA | |

GATE TRIGGER CHARACTERISTICS AND RATINGS

| Symbol | Parameter | Test Conditions | Max. | Units |
|-----------------|--------------------------|---|------|-------|
| V _{GT} | Gate trigger voltage | V _{DRM} = 5V, T _{case} = 25°C | 1.5 | V |
| V _{GD} | Gate non-trigger voltage | At 50% V _{DRM} , T _{case} = 125°C | 0.4 | V |
| I _{GT} | Gate trigger current | V _{DRM} = 5V, T _{case} = 25°C | 400 | mA |
| I _{GD} | Gate non-trigger current | At 50% V _{DRM} , T _{case} = 125°C | 15 | mA |

CURVES

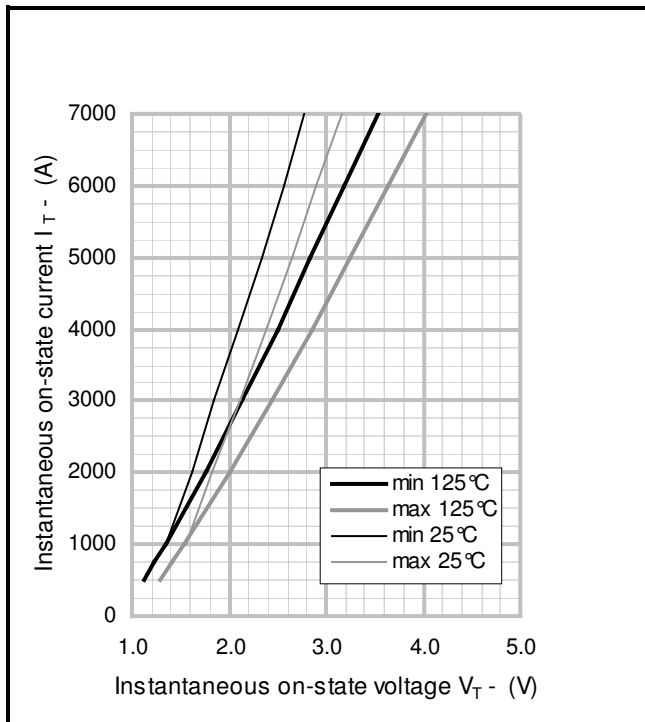


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.907134
 B = -0.011004
 C = 0.000304
 D = 0.012936

these values are valid for T_j = 125°C for I_T 500A to 7200A

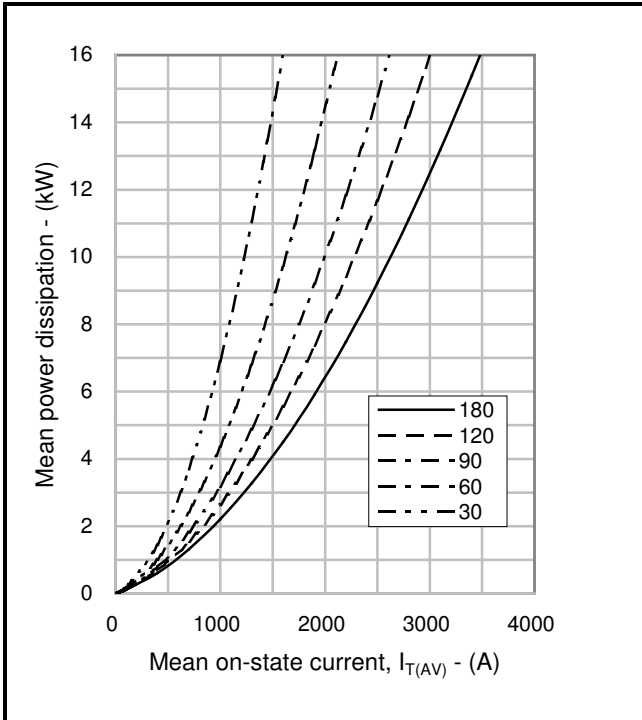


Fig.3 On-state power dissipation – sine wave

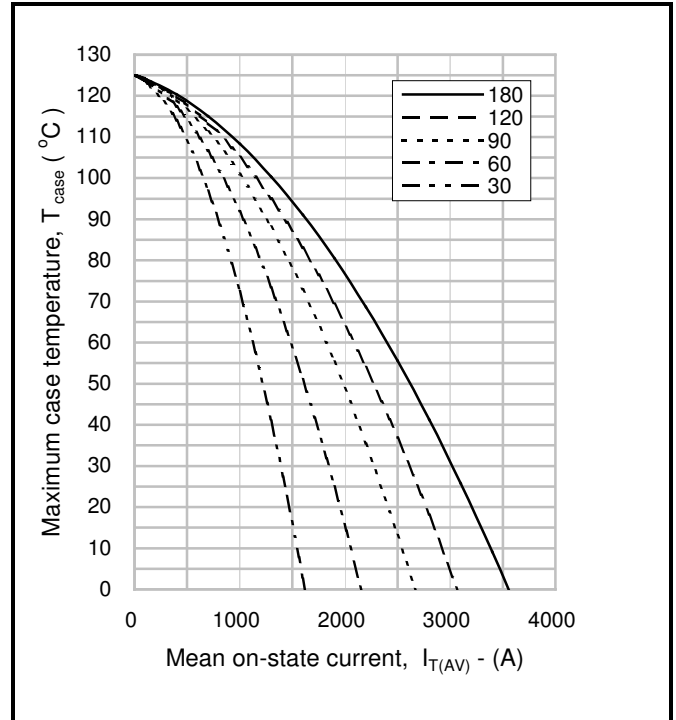


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

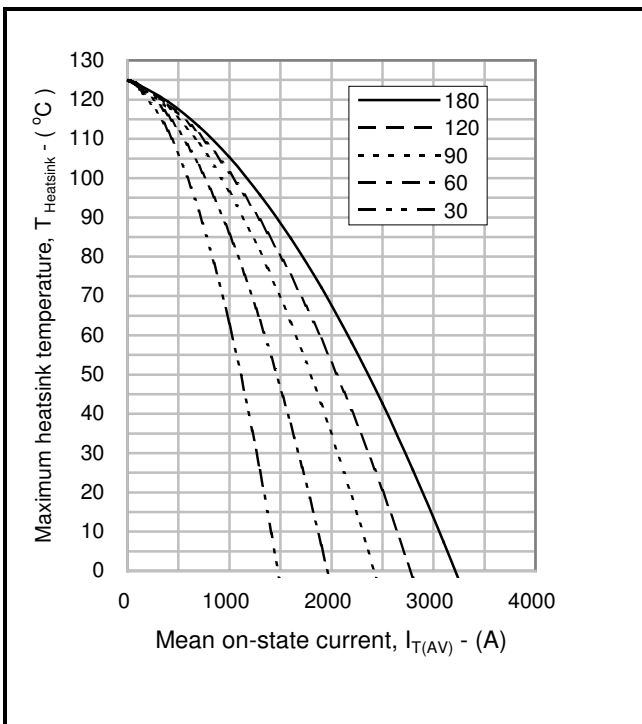


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

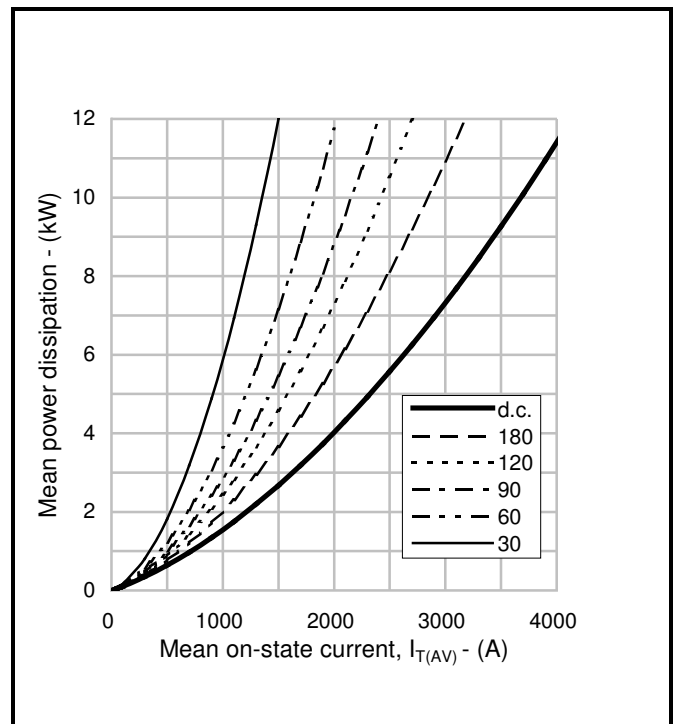


Fig.6 On-state power dissipation – rectangular wave

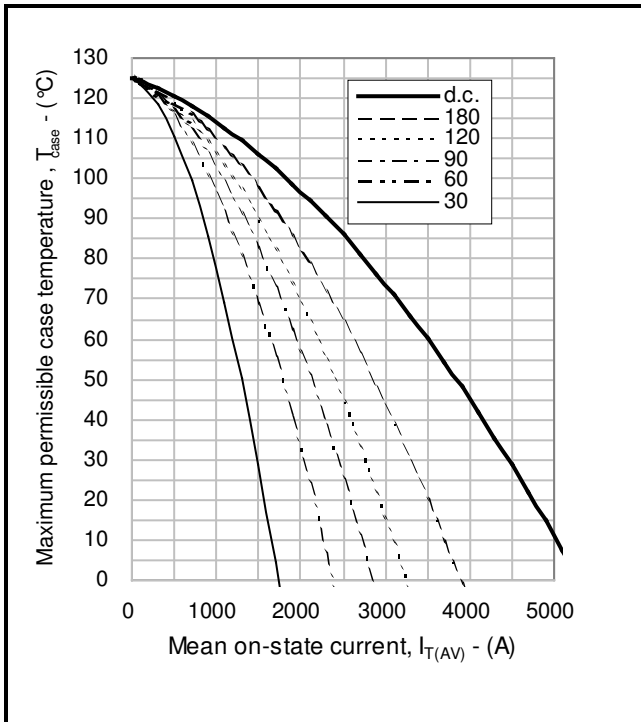


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

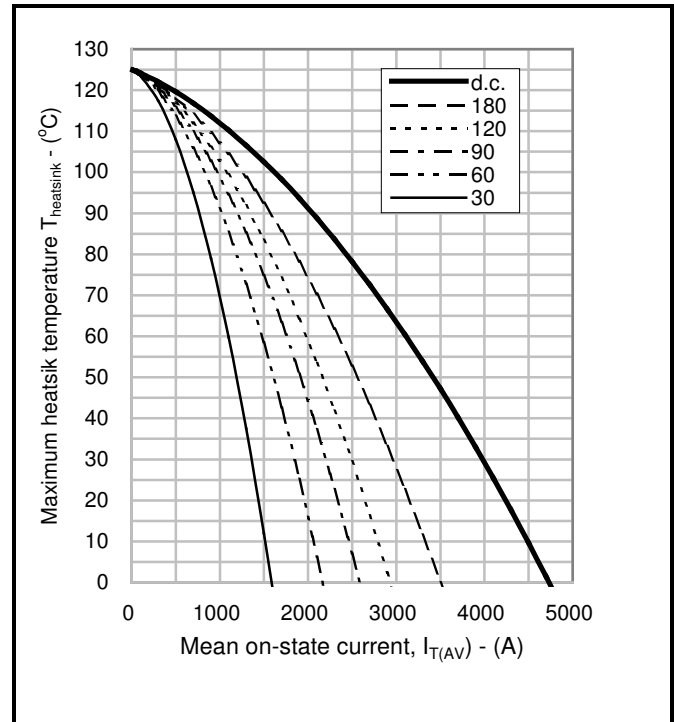


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

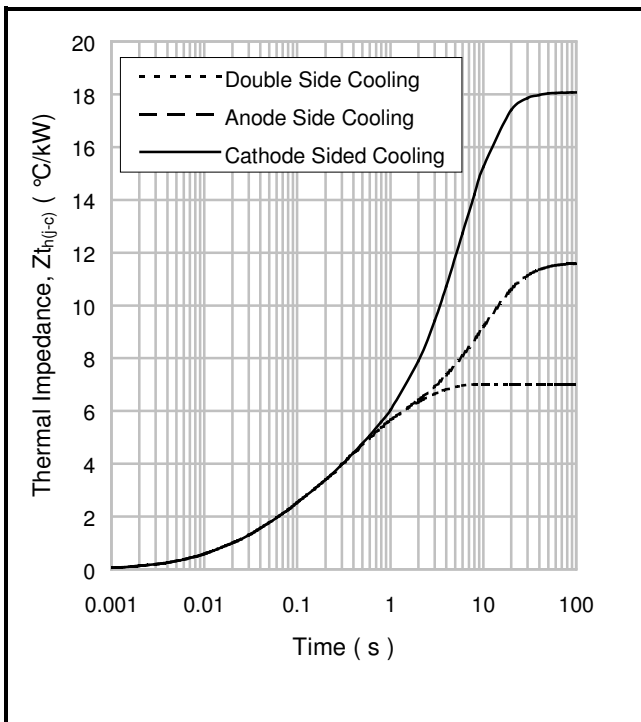


Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

| | | 1 | 2 | 3 | 4 |
|---------------------|------------------------|-----------|-----------|-----------|--------|
| Double side cooled | R _i (°C/kW) | 0.502 | 1.333 | 2.9559 | 2.2335 |
| | T _i (s) | 0.0137081 | 0.0548877 | 0.3311925 | 1.6905 |
| Anode side cooled | R _i (°C/kW) | 1.3035 | 3.138 | 1.1859 | 5.9136 |
| | T _i (s) | 0.0251065 | 0.2410256 | 1.0806 | 11.002 |
| Cathode side cooled | R _i (°C/kW) | 1.2616 | 2.6216 | 13.3603 | 0.8304 |
| | T _i (s) | 0.0245837 | 0.2005035 | 5.7854 | 16.765 |

$$Z_{th} = \sum [R_i \times (1 - \exp.(-t/t_i))] \quad [1]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

| Double side cooling | | | Anode Side Cooling | | | Cathode Sided Cooling | | |
|---------------------|---------------------|-------|--------------------|---------------------|-------|-----------------------|---------------------|-------|
| α° | $\Delta Z_{th} (z)$ | | α° | $\Delta Z_{th} (z)$ | | α° | $\Delta Z_{th} (z)$ | |
| | sine. | rect. | | sine. | rect. | | sine. | rect. |
| 180 | 0.70 | 0.48 | 180 | 0.67 | 0.47 | 180 | 0.67 | 0.47 |
| 120 | 0.80 | 0.68 | 120 | 0.77 | 0.66 | 120 | 0.77 | 0.66 |
| 90 | 0.90 | 0.78 | 90 | 0.87 | 0.75 | 90 | 0.87 | 0.76 |
| 60 | 1.00 | 0.89 | 60 | 0.95 | 0.86 | 60 | 0.95 | 0.86 |
| 30 | 1.07 | 1.01 | 30 | 1.02 | 0.96 | 30 | 1.02 | 0.96 |
| 15 | 1.10 | 1.07 | 15 | 1.05 | 1.02 | 15 | 1.05 | 1.02 |

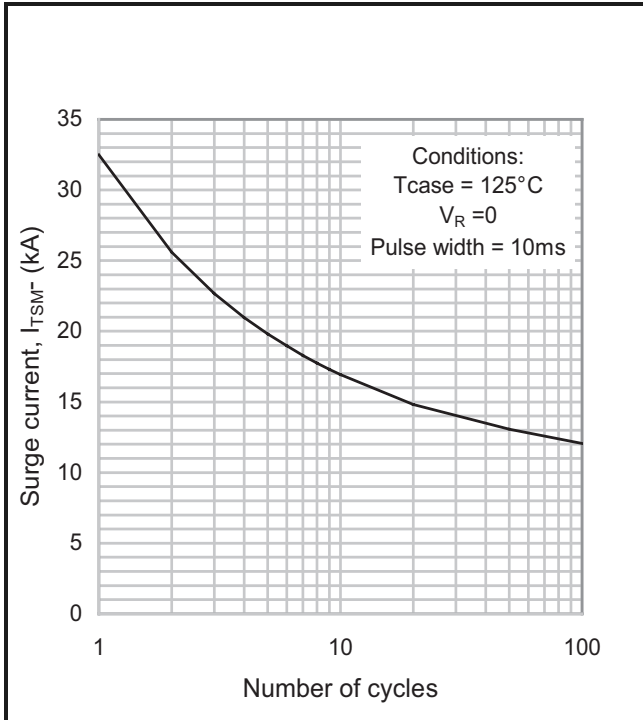


Fig.10 Multi-cycle surge current

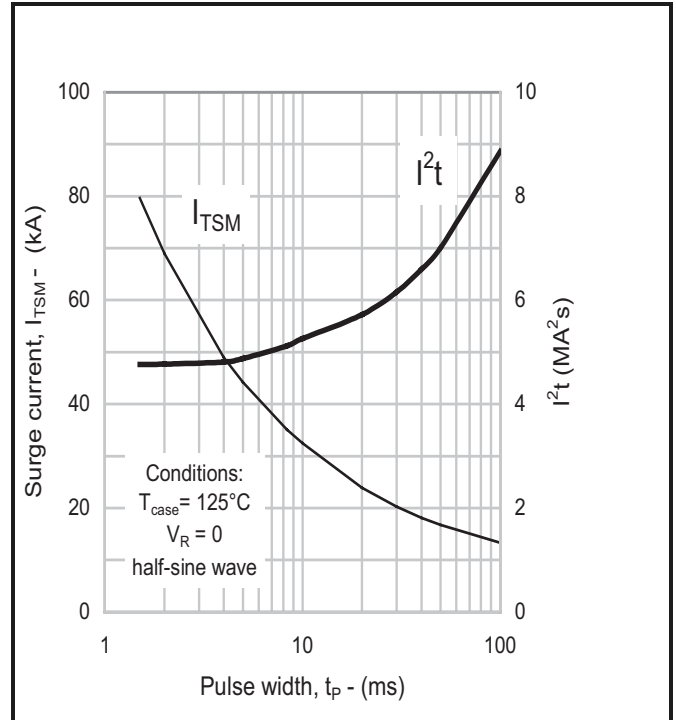


Fig.11 Single-cycle surge current

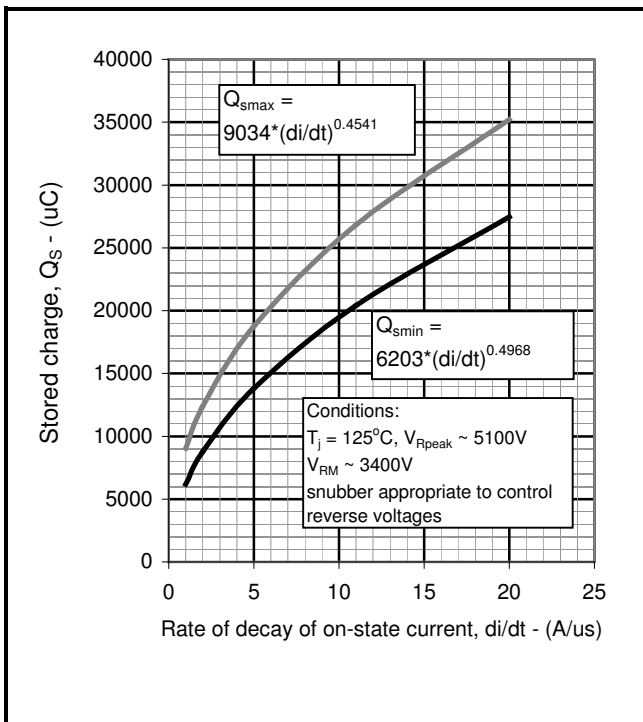


Fig.12 Stored charge

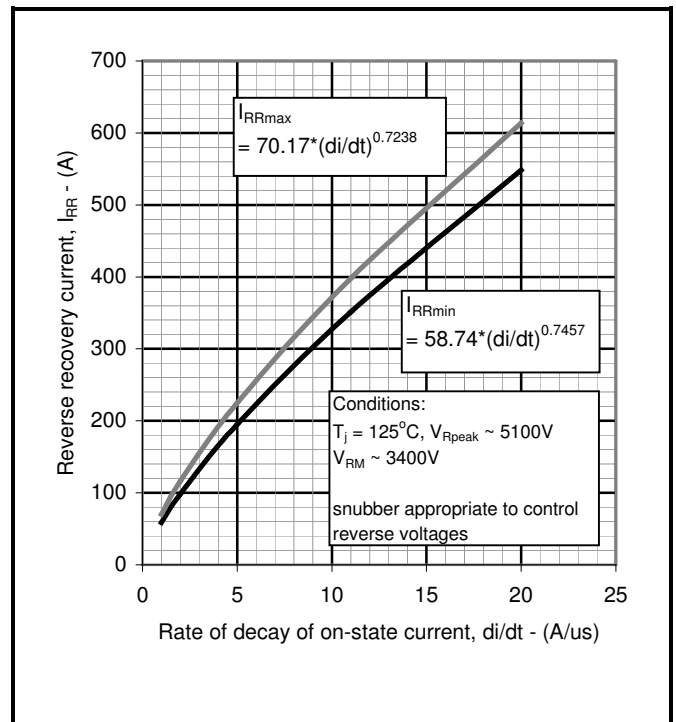


Fig.13 Reverse recovery current

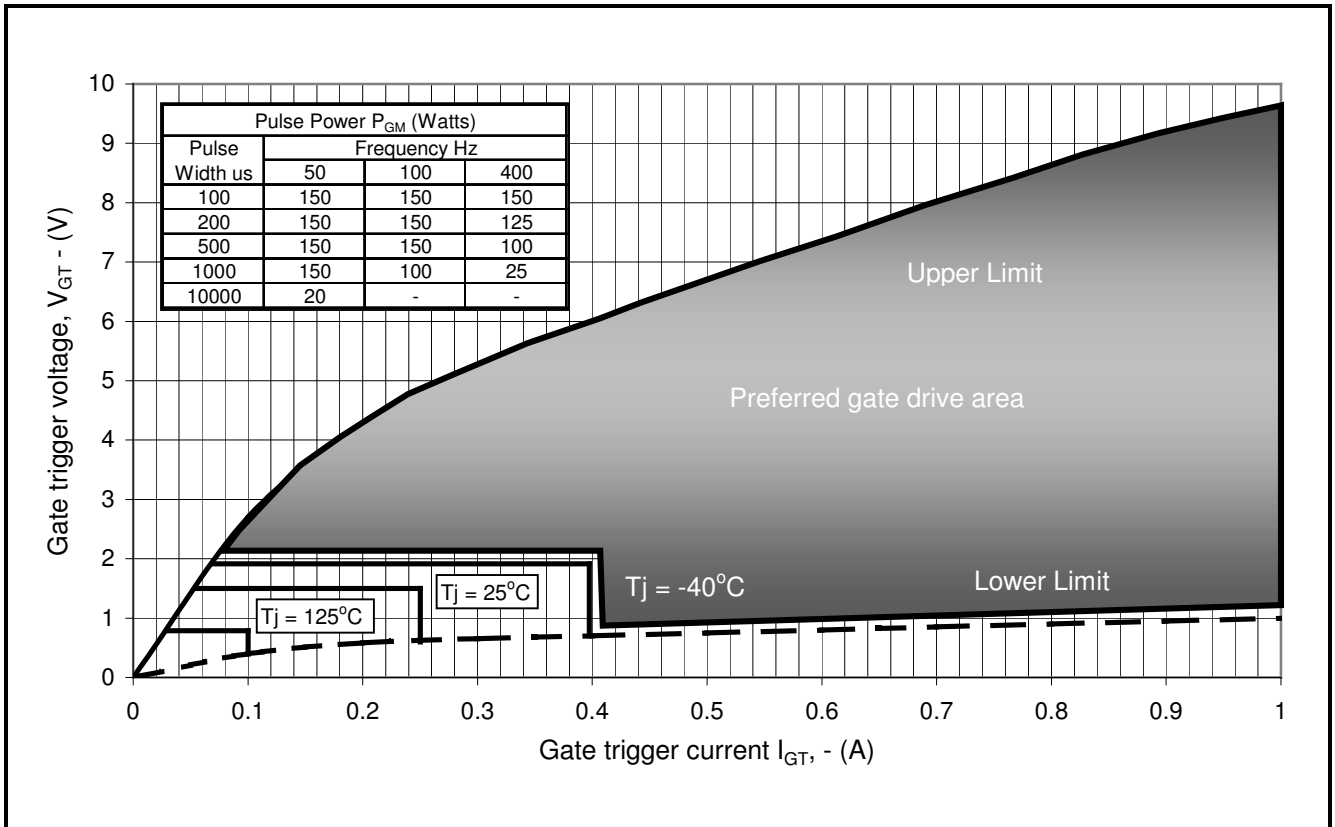


Fig14 Gate Characteristics

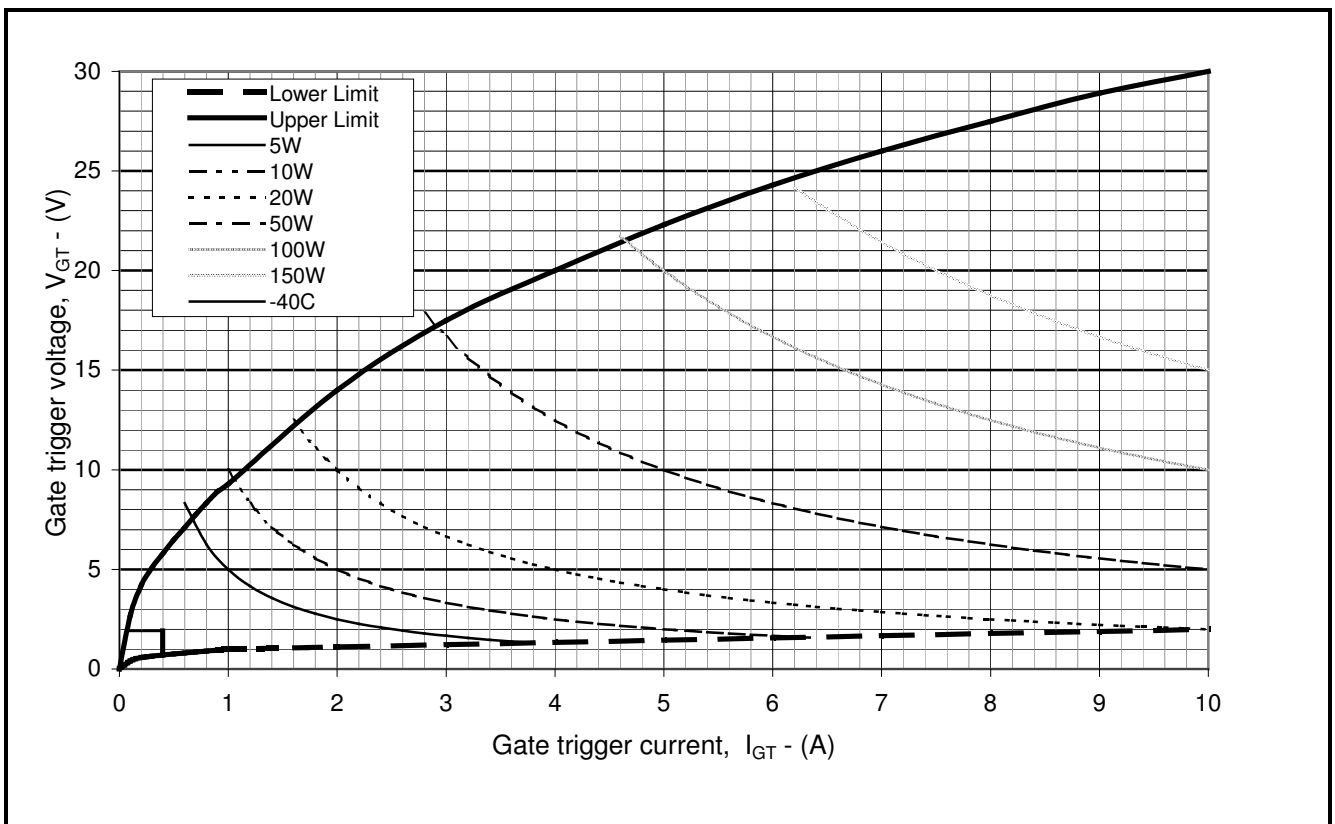


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

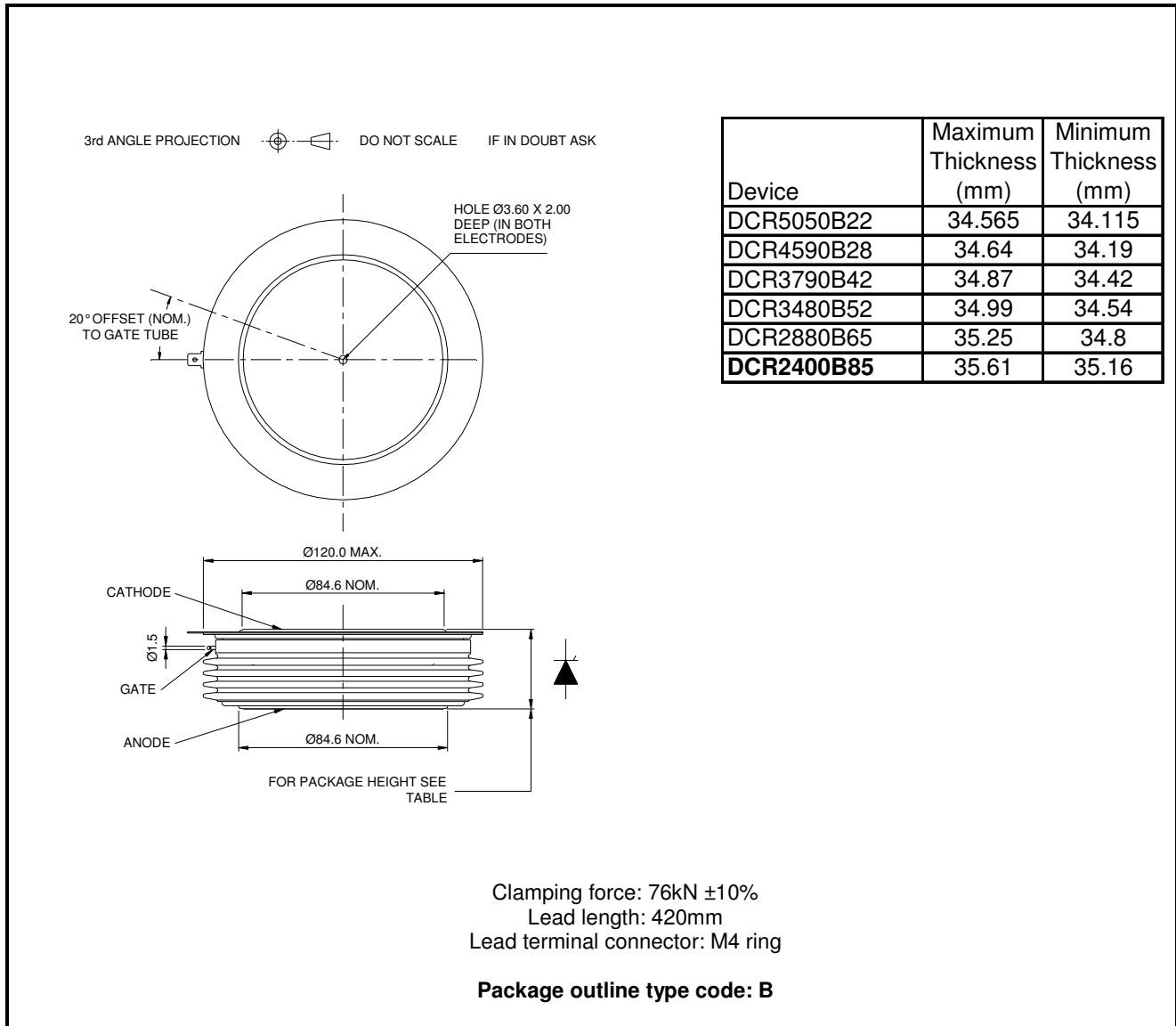


Fig.16 Package outline

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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